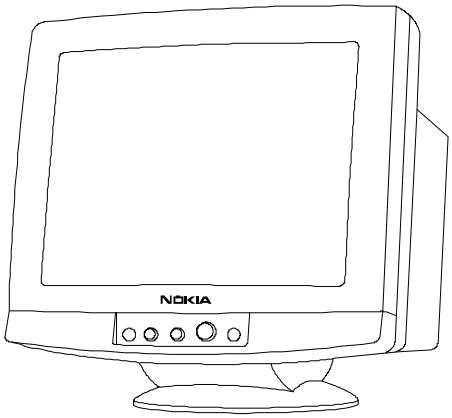
Circuit Description

	Chassis 445T

21” Color Monitor



Circuit Description
Circuit Diagrams

When re-ordering manuals, please quote the model name and part number.	**ZB1574** 08.97

1. Introduction

1.1 General features

This device is an autosync type microprocessor controlled 21" monitor. It has a line frequency range of 30…121 kHz and vertical frequency range of 50…150 Hz, with a maximum resolution of 1800 x 1440. The monitor has been designed to operate with separate TTL-level horizontal and vertical sync pulses (H- and V-sync), composite sync, and sync on green- sync pulses.

The monitor operates with a mains voltage range of 90…264 VAC 50/60 Hz. The monitor power supply has been designed to function on the whole frequency range, so there is no need for a separate voltage switch.

The monitor has VESA standard power save modes (VESA Power Save).

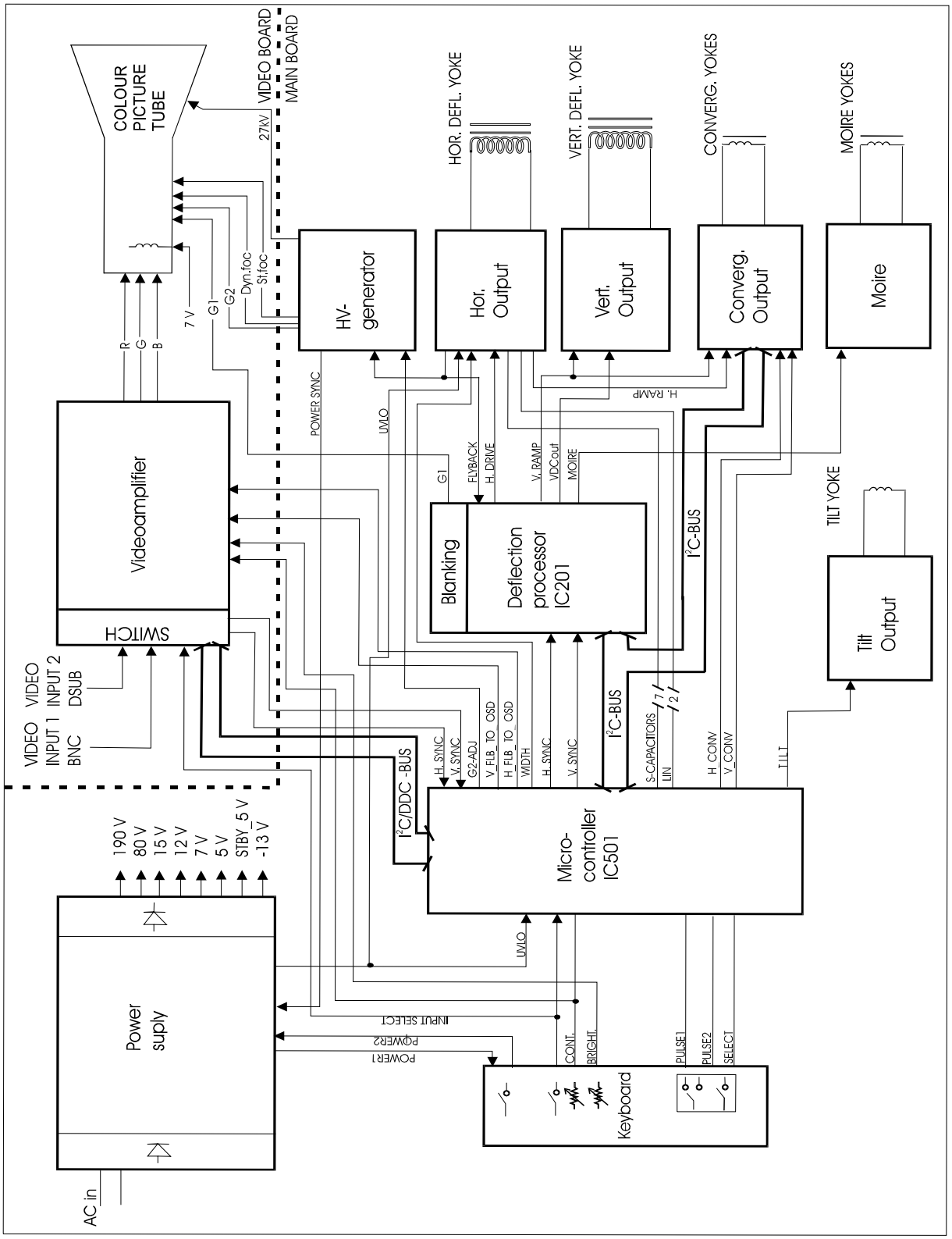
The rotating selector in the monitor front panel is used to display different menus on the screen. The menus are used to adjust various picture properties, for instance picture size, geometry, colour temperature etc.

The monitor recognizes the used mode according the vertical and horizontal sync pulses frequency, and the vertical sync pulses polarity. If a memory location has been created for the mode, meaning that the monitor manufacturer has pre-adjusted the mode in question, the picture size and geometry are automatically optimized. If the monitor does not recognize the used mode, the mode has not been optimized, and the user can easily adjust the picture by using the rotating selector. The adjusted values are saved in the monitor's memory for subsequent use.

The monitor does not have a mains switch to disconnect the supply voltage. The power switch in the front panel switches off the monitor's power supply, at which time all secondary voltages decrease, but primary filter capacitors C113 and C114 are still connected to mains voltage.

1.2 Block diagram

The monitor power supply and deflection part block diagram is illustrated in picture 1. It contains the following operating blocks:



picture 1

1.2.1 Power supply

The power supply generates the voltages needed by the monitor. It contains also the VESA Power Save and picture tube demagnetization functions. The operation frequency is synchronized to horizontal deflection frequency.

1.2.2 Deflection driver

In view of the incoming sync pulse, the deflection driver generates a correctly timed control signal to the line output stage. The driver monitors the line output stage function (F_LIMIT). It controls also the vertical output stage and generates vertical frequency picture geometry correction voltages, as well as the vertical frequency control voltage for the dynamic focus. The driver controls the high voltage and the screen blanking during a mode change situation.

1.2.3 High voltage generator

Generates a regulated 27 kV high voltage, as well as a focus- and G2-voltage. Synchronizes the power supply.

1.2.4 Vertical output stage

Generates proper current for the vertical deflection coil.

1.2.5 Line output stage

Generates the current needed by the line deflection coil, the DC-current for the frame centering, as well as the linearity- and S-correction. The line fly-back pulse (FBP) generated by the stage is used to control the high voltage generator and the deflection driver, and to generate the horizontal blanking pulse.

1.2.6 Blanking circuit

Generates the vertical- and horizontal fly-back pulses, and controls the picture blanking and narrowing in mode change situations. When the monitor is switched off, the circuit prevents the appearing of white spot.

1.2.6.1 Other functions

These auxiliary functions are for instance:

1. The beam current limiter circuit, which limits the maximum beam current to the required level.
2. The TCO-compensating circuit, which generates a TCO-compensating pulse, used to decrease the magnetic field sent forward by the monitor.
3. The reset circuit, which generates the reset-pulse needed by the processor. It also generates a reset-pulse in a picture tube cross-over situation, thereby reducing the risk of a processor failure.
4. The clamp pulse circuit, which generates the black level clamp pulse needed by the video.
5. The Moiré adjustment circuit, used to decrease the Moiré in the picture frame.
6. The demagnetization circuit, used to remove the magnetism from the metal components of the monitor.

1.2.7 DDC

The Display Data Channel or DDC is a two-way data transfer channel between the monitor and the computer. It can be used for instance to transfer data about the monitor properties, as the maximum refreshment frequency, in order for the computer to automatically take advantage of the monitor's performance level.

1.2.8 The microprocessor

Controls all the monitor functions according the horizontal- and vertical frequency, as well as the user's commands.

1.2.9 Video amplifier

Amplifies the approx. 0.7V RGB-signals coming from the video card through the signal cable to approx. 45V control pulses suitable for the picture tube.

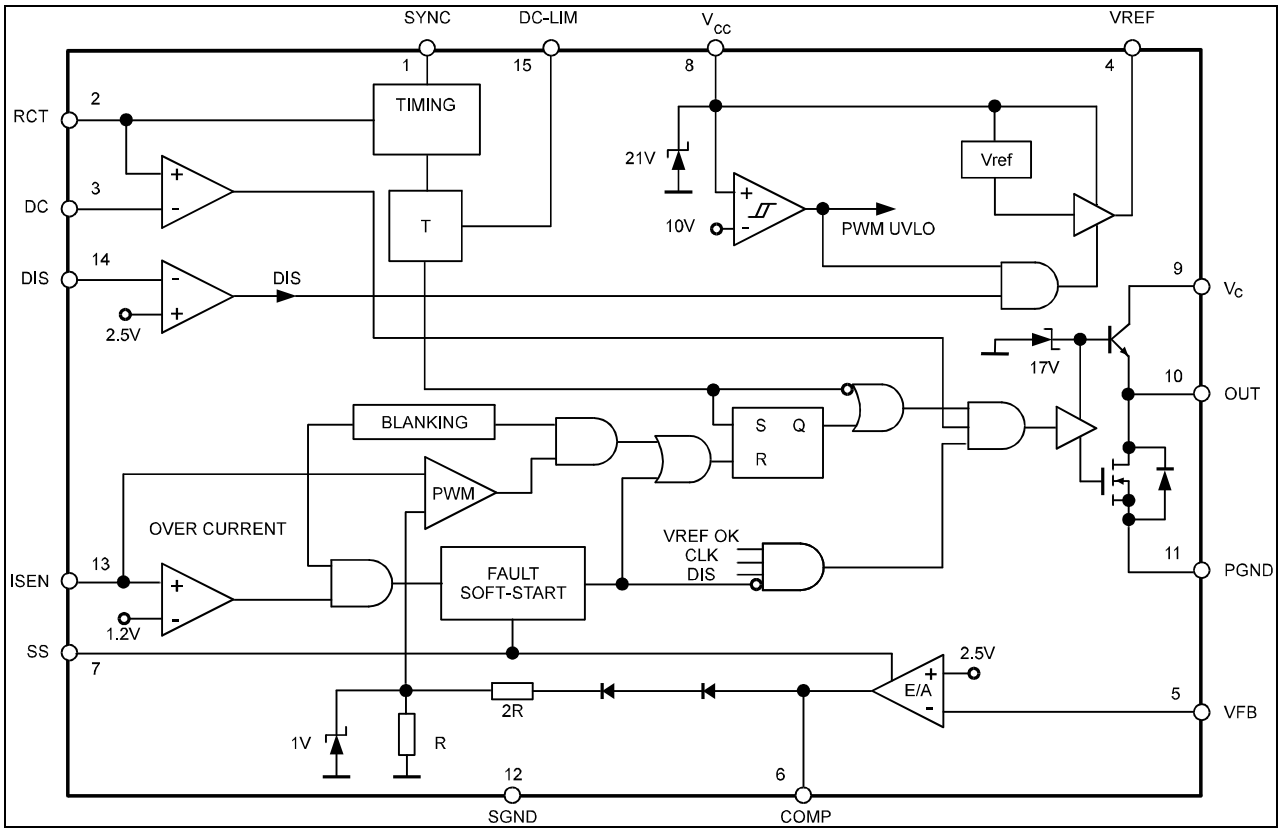
2. Power supply

2.1 General features

The voltage supply is a secondary regulated, current-shaped, continuous-/non-continuous Fly-back/Forward type switch mode power supply, with an operating voltage range of 90…264 VAC.

The regulation from the secondary is realized with an opto isolator. The operating frequency (switch mode frequency) is 14…121 kHz and is synchronized to line frequency. The power supply operates on a non-continuous function mode with low primary currents and shifts to continuous mode when the load is increasing.

The voltage supply is based on the SGS-Thomson IC circuit L4990 (current mode PWM). The circuit block diagram is illustrated in picture 2.



picture 2

The power supply control circuit L4990 is based on the popular UC3842 circuit, which contains a differential amplifier, an RC oscillator, a current sense comparator, a 5V reference voltage, an output stage for the FET control, and an under voltage lockout. In addition to the previously described UC3842 functions, the circuit has also an adjustable Soft start function, a two stage over current protection, a pulse ratio limiter circuit (not used in this monitor, since the maximum pulse ratio has been adjusted to 100%), and an over voltage disable function. A more reliable function of the power supply in various failure situations has been acquired with these functions.

2.2 The start-up

The mains voltage is rectified with diodes D101…D104 and filtered with capacitors C113 and C114. After the power switch has been pressed down, T101 gets base current through resistors R104/108 and starts to lead. As a result, C118 starts to charge and the voltage in point IC101/8 increases. When C118 voltage has increased to 16V, the IC101 under voltage lockout lets the circuit start up. Simultaneously, the

oscillator starts to operate and T105 goes leading. The (soft start) capacitor C129 starts also to charge with constant 20uA current.

The current through mains transformer M104 primary coil (pins 2 and 10) and T105 increases, until the voltage loss over current sense resistors R130-132 is equal to the soft start capacitor (C129) voltage, which limits the output voltage of the internal current sense comparator (E/A in the block diagram). At that point, the current sense comparator sets T105 to off mode and the energy stored in the primary coil is transferred to secondary coils and forwarded to the secondary capacitors through the secondary diodes. At that point, IC101 oscillator directs T107 to lead etc.

The soft start capacitor voltage is continuously increasing, so the pulse ratio is also increasing, and the current through the primary coil increases with every sequence. Since the pulse ratio is very low at the beginning of the start-up, the secondary voltages increase slowly. When the soft start capacitor is charged to its maximum, the soft start circuit will not limit the power supply function. IC101 oscillator redirects T105 to lead etc. This is repeated as long as the secondary capacitors have been charged to the proper voltage level. At that time, the feedback from the secondary starts to control the IC101 differential amplifier, which is still in control of the primary current through T105 (explained in 3.4 voltage regulation).

When IC101/4 (Vref) voltage has increased (5V), T101 stops leading. Simultaneously, T103 starts to lead and switches additional energy to the circuit through auxiliary coil M104/14. When the circuit runs in normal mode, D108 anode has a higher potential than D107's, and the circuit takes its power from supply voltage coil M104/20. The circuit gets its supply voltage from the auxiliary coil also in Power-off mode.

Right in the beginning of the start-up situation, T106 is directed leading, and prevents IC101 from running on an excessively low base frequency. A low frequency and a simultaneous overload in the secondary (empty capacitors) would produce audible sound in the M104.

If the IC101 supply voltage drops under 10V (a power blackout for instance), the internal under-voltage lockout disconnects the circuit, and the start-up sequence is restarted.

2.3 Synchronizing

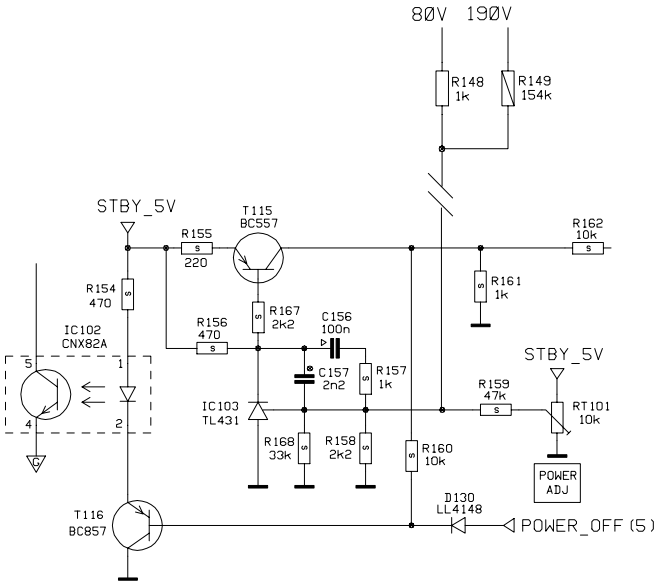
The power supply is synchronized to line deflection frequency. The synchronizing is taken inductively from the high voltage stage with M103. A sufficient signal amplitude is achieved with one wire loop around the ferrite. The pulse is adjusted to the circuit with R118 and DZ101. The rising pulse edge always synchronizes the IC oscillator, which in turn commands T105 to lead. With this method, the power supply runs with the same frequency as the line output stage and the high voltage generator. The power supply oscillator free oscillating frequency is adjusted with components R115, R116 and C127, which define the power supply oscillating frequency when the deflection stage is not operational (for example a Power off situation). This free oscillating frequency is approximately 14 kHz. The sound disturbance mentioned in the start-up section will not be generated, since the secondary charge is low.

2.4 Voltage regulation

The voltage feedback data is taken from a 190V voltage, which is decreased to the IC103 regulator reference voltage level of 2.5V with R149, R158, and R168. Regulator IC103 is composed of an inverting amplifier and a reference voltage.

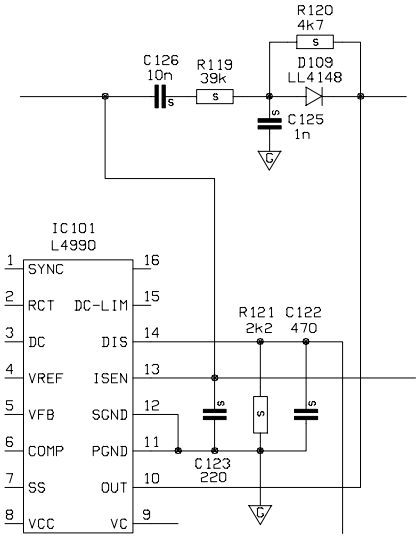
Function example:

If the 190V voltage tends to rise (the charge is decreasing), IC103 grid voltage increases, at which point the current through IC103 and R156 increases. This current increases the R156 voltage loss, at which time T115 starts to lead and T116 starts to close. As a result, the current flowing through IC102 diode (opto) is decreasing. At that time, IC102 transistor's and R109 current is decreasing, and IC101/5 (differential amplifier negative input) voltage is rising and the differential amplifier output voltage is decreasing. The differential amplifier output voltage functions as the reference voltage of the current sense comparator, at which time the comparator decreases the primary current, thereby resulting in the decrease of the 190V secondary voltage.



2.5 Slope compensating

Since the primary current pulse ratio can be over 50%, the IC101 circuit contains a slope compensation in order to ensure the stable function of the power supply in all circumstances. A saw tooth wave is generated with R120, C125 and D109 from T105 control. The wave form is summed through R119 and C126 to the input voltage of the current sense comparator (IC101/13). The active sum signal in the current sense is altering the primary current switch off value in order to stabilize the adjustment loop.



2.6 Over current monitoring

Circuit L4990 contains an over current disable function circuit, which in failure situations prevents the secondary voltages from increasing excessively. In a failure situation, the electrolyte capacitors and other secondary components could be damaged.

In a normal situation, when the secondary 190V voltage is at the right level, IC101 supply voltage is approximately 16V. At that time, IC101/14 (DIS) voltage is approximately 2V through resistors R122, 121 and C122. If the regulation is not operating and the secondary voltages increase excessively, IC101/14 voltage is simultaneously increased. When it reaches 2.5V, T105 control goes down and IC101 oscillator is shut down. It must be noted that R122, 121 and C122 time constant is very small. As a result, every running sequence can be observed separately. Even one sequence over 2.5V could disconnect the supply power function. In an over voltage situation the monitor power supply is completely shut down and the secondary voltages decrease, thereby preventing the voltages from rising dangerously high even briefly.

Since the IC is restarting in an over voltage situation only after its supply voltage has dropped under 10V, the situation can be resolved only by disconnecting the circuit supply voltage with the power switch for approx. 3 minutes (at which time C113, 114 and C118 voltage is discharged).

2.7 Primary current limiter

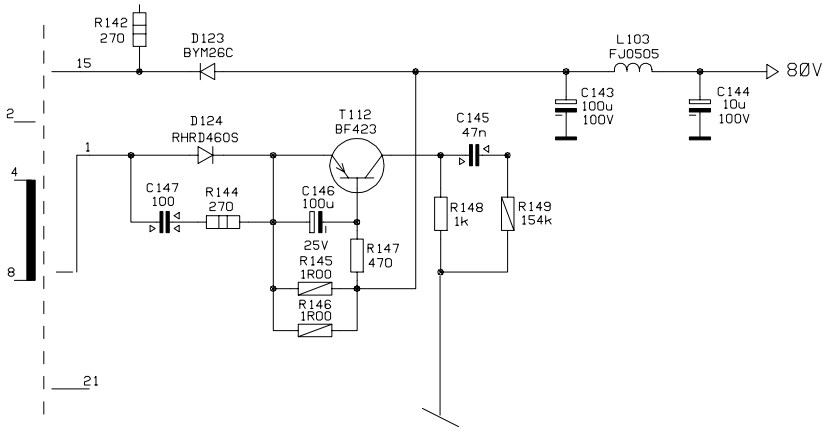
The circuit has a two stage primary current sense and protection function. When the power supply is functioning normally (R130, 131 and 132 maximum pulse voltage is approx. 1V), the feedback data from the secondary controls the primary switch pulse ratio through the current sense comparator, and furthermore the secondary voltages. The voltage regulation functions as described previously.

When an overload situation occurs and the primary current increase leads the current sense resistors (R130-132) voltage over 1.2V, the circuit over current protection function is enabled. At that time, the circuit disconnects immediately primary switch T105 control and discharges soft start capacitor C129. C129's charging time to 5V defines the next time period when the primary switch is directed leading. If the overload situation is still continuing, the primary switch is immediately opened when the current sense resistors voltage loss is over 1.2V. In consequence of C129 time constant, the circuit controls the primary switch with a very low pulse ratio in a failure situation.

In this kind of continuous overload situation (for instance a secondary side component short circuiting) only a very small amount of power is transferred to the secondary. This prevents the overheating of the overloaded component, thereby preventing any further damage. If the overload situation was only temporary (for instance a failure occurring in a mode change situation), the monitor keeps functioning, without even noticing the user.

2.8 Secondary current limiter

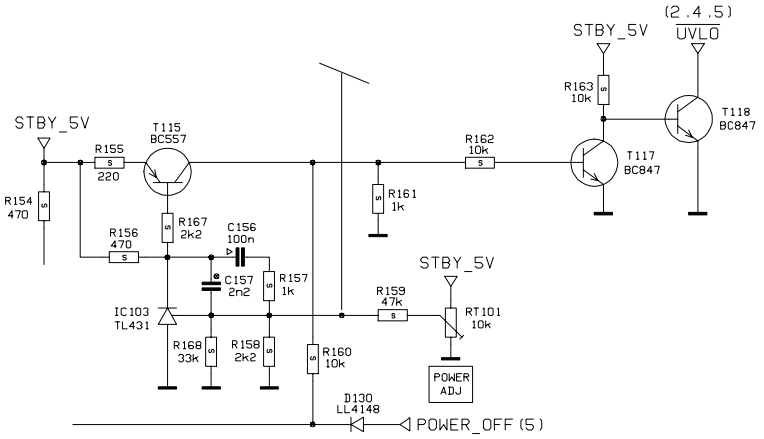
Since the 190V and 80V secondary coils are serial, both voltages current flows through R145 and R146. In an overload situation the voltage loss of these resistors increases over 0.7V, at which time T112 starts to lead and give extra current to the feedback voltage data through R148. At that point, regulator IC103 grid voltage increases, and due to feedback, the power supply output voltages decrease as well. The lower secondary voltages are protected from overload with a non-flammable resistor or fuse.



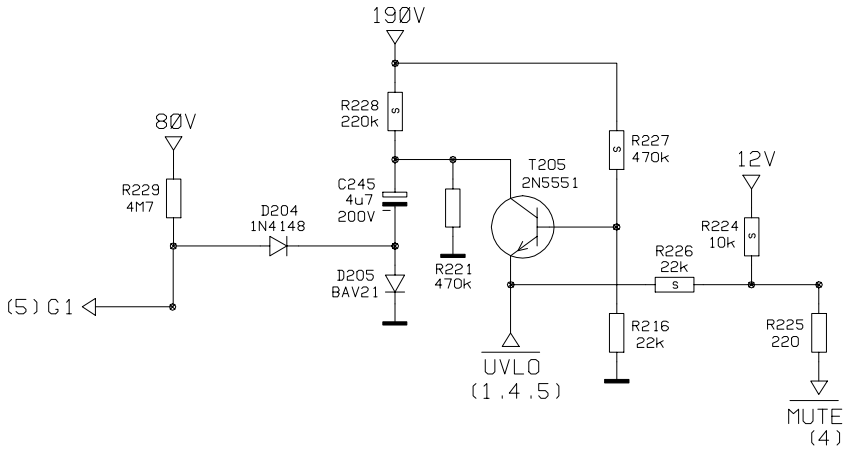
2.9 UVLO-signal

The UVLO-signal (transistor T118) is used to ensure the reliable function of the line deflection and high voltage generator. The UVLO-signal is activated when the power supply is started or shut down, at which point the produced voltages have undetermined values.

When starting up, STB_5V increases rapidly and T118 is kept leading through R163. When the power supply is starting to run on normal voltages, T117 switches T118 non-leading, at which time the UVLO signal is deactivated. When shutting down, the feedback voltage data comands T115 non-leading, at which point T117 closes down and the UVLO signal is activated.



When the UVLO-signal goes down, T205 emitter connects to the ground. Simultaneously, C245 positive end connects to the ground, resulting to a negative blanking pulse on the G1-line, preventing a white spot from appearing when the monitor is shut down.



Width driver IC401/1 connects also to the ground through T118 and D402, resulting to the disconnection of the line deflection stage power feed. Deflection driver IC201 still gets supply voltage (12V is decreasing, but is still high enough for the driver to function) and gives an H-drive signal to transistor T409 of the line deflection output stage. During this sequence, line deflection output stage transistor T409 discharges the S-capacitors. This prevents the line deflection stage from starting up with an excessively high supply voltage (S-capacitor voltage) in the next starting sequence.

Since the high voltage generator function is synchronized to the fly-back pulse coming from the line deflection output stage, the generator is shut down simultaneously with the line deflection stage.

3. Power Save -function

The monitor can be controlled to various “VESA Power Save Management”-standard power save modes, by removing the field- and/or line synchronization going to the monitor. The processor monitors the sync pulses and performs the needed actions. The power consumption caused by the beam current is decreased with contrast adjustment, and the line output stage losses by adjusting the picture width.

The led, situated in the user panel, shows the current power supply mode. The twin colored led has two anodes and a cathode. The colors are red and green. The red’s anode is connected through D601 to STBY_5V, the green’s anode to the heater voltage, and the common anode through R601 to ground level.

In **Power on** -mode the monitor functions normally and all voltages are connected. Since the green anode is connected to heater voltage (approx. 7V), the common cathode voltage exceeds 4V. As a result, only the green led is glowing, since the red led treshold voltage is not exceeded.

The mode is transferred to **Stand by** if the monitor does not get any line sync. The processor generates a line sync, which in this case is approx. 80 kHz. Simultaneously, the contrast is directed to minimum, at which point the screen is black. The led is green.

The mode is transferred to **Suspend** if the monitor does not get any field sync. In addition to “stand by” controls, the processor comands the suspend voltage to 0V. As a result the IC105 regulated 12V is disconnected. At that point, IC201/203/301/401 functions are disconnected and the monitor shuts down almost completely. The voltage supply does not get sync either and transfers to a lower operational frequency. The secondary voltages regulation is still operational. The green led is lit, since the 7V is still connected.

In suspend-mode the power consumption is remarkably low compared to power on mode, typically approx. 24W.

The mode is transferred to **Power off** mode if the monitor does not get neither line nor field sync. In addition to suspend controls, IC501/15 (power-off) voltage increases to 5V. T116 stops leading, at which time the feedback voltage data is disconnected and the secondary voltages decrease. The red led is lit, since the 7V has been disconnected.

At that point, the monitor power consumption is approx. 3W.

In order for the monitor to be started up from Power off mode, STBY_5V voltage feed must be secured. A 190V secondary voltage (approx. 12V in Power off mode) is used for this purpose, from which is regulated an input voltage to IC106 through DZ103 and T113. In normal run (Power on) the T113 source is in higher potential than the grid, resulting to a situation where no current is flowing through T113.

4. Deflection driver

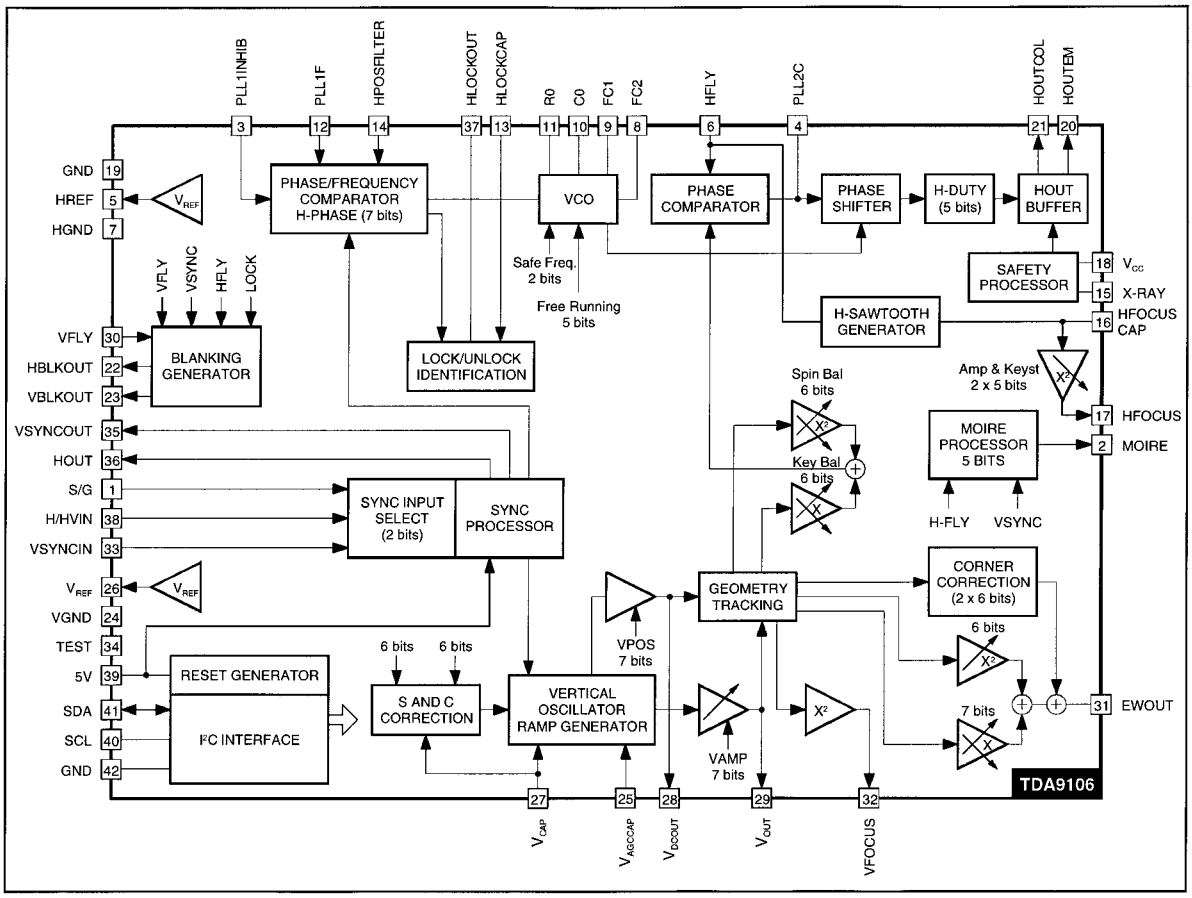
4.1 General features

The used deflection driver is a SGS-Thomson TDA9106 circuit. The circuit is based mostly on the older TDA9105 circuit. The main difference is in the circuit functions control, which has been altered from analog voltage control to I^2C bus control.

The circuit contains the needed blocks to control both horizontal and vertical deflection. In addition are found the essential functions for the picture geometry correction controls. Picture corner area correction has been added to the geometry adjustments. Other functions are the x-ray block circuit, the under voltage lockout, the blanking output and the vertical frequency parabola for the dynamic focus control. The circuit operation frequency range is 15-125 kHz and the supply voltage range 10-13.2V. The circuit is packed in a 28-pin DIP-box.

4.2 Block diagram

The TDA9106 block diagram is illustrated in picture 3.



picture 3

Three separate operation field blocks can be distinguished in the block diagram: the line frequency blocks, the field frequency blocks and the I^2C-interface block. The line frequency blocks generate the H-drive signal to the line deflection output stage. The field frequency blocks generate a control voltage to the vertical deflection output stage as well as the picture geometry correction voltages. The I^2C block is used to control the circuit functions and its parameters. In addition, the circuit has common blocks for line and field frequency components, like the blanking block and the protection block or “safety processor”.

4.2.1 Line frequency blocks

The line frequency blocks form two successive phase locks: PLL1 and PLL2.

PLL1 is composed of a phase/frequency comparator and a VCO.

The comparator keeps the VCO frequency at the same level as the incoming sync pulses frequency. The saw tooth wave (IC201/10) phase generated by the VCO is proportionally adjustable to the incoming sync pulses. The adjustment value can be between 0 and 128 (7 bits). The circuit has been designed to generate an adjustment voltage from the digital value with the D/A converter. When the voltage is 4V, the fly-back pulse mid position is lagging 10% behind the sync pulse front edge. The whole adjustment range (2.8…4V) is +-10%.

The PLL1 phase comparator function can be prevented with a positive voltage brought from IC201/3 (PLLINH). At that point, the VCO frequency is not dependent from the incoming sync pulses. In this circuit, a V_SYNC signal has been connected to the point, to prevent the comparator failure during the field synchronization.

This procedure is also used with a composite sync signal, at which time undesirable sync pulses or levels might occur in the H_SYNC line during the field sync pulse, causing phase comparator failures.

PLL1 also contains a clamp detector, which indicates if the phase lock is clamped to the incoming sync signal or not. If the phase lock is clamped, voltage IC201/37 (H-Lock cap) is high (over 6.5V), at which time IC201/37 is directed with the internal reference (6.5V) to 0V. Correspondingly, if the phase lock is not clamped, IC201/13 voltage drops under 6.5V and IC201/37 rises to +5V.

Phase detector PLL2 compares the line fly back pulse at IC201/6 and VCO phase. If the fly-back pulses phase tends to alter in relation to the VCO phase for instance during a deflection processor heat drifting, the output voltage IC201/4 of the phase detector is altered, which in its turn alters the decision levels of the circuit's internal comparators, thus restoring the H_Drive signal phase and fly-back pulses phase to the appropriate level. Phase lock 2 is thereby compensating the various delays generated in the horizontal deflection output stage. The maximum adjustment value is 33.75%.

The actual H_Drive signal obtained from either IC201/20 or /21. 20 is the output transistor emitter and 21 is the collector. The H_Drive signal pulse ratio can be adjusted through the I^2C bus. The adjustment range is 30%…60% (5 bits). When starting up, the pulse ratio is automatically directed to 60%, thereby preventing extra exertion to the line output transistor.

4.2.2 Field frequency blocks

The vertical part of the circuit contains a vertical oscillator which is synchronized with vertical pulses (IC201/33). It generates a ramp voltage, used to control the vertical output stage. From this same ramp voltage are also generated with multipliers and summing circuits the picture geometry correction signals. When generating the ramp voltage, the circuit's external components are integration capacitor C225 and level adjustment capacitor C228. This capacitor is used to keep the ramp amplitude constant regardless of the frequency. The ramp wave is obtained from IC201/29. Its amplitude and phase can be adjusted through the I^2C bus (7 bits).

If the ramp was completely linear, the picture center would be narrower in relation to the upper and lower edge. By adding S-correction to the ramp, the picture is rendered linear. In addition, linearity error could occur in some vertical output stages, at which time the picture upper half is not as high as the lower half. This error can be corrected with C-correction. Similarly with amplitude and phase, also S- and C-correction is adjustable through the I^2C bus.

The geometry correction signals are also generated from the ramp generator ramp. The E/W parabola is generated from the vertical ramp with an analogy multiplier and a current transformer. The vertical is first brought to the multiplier, which squares the ramp, thus generating a parabola voltage. The parabola is then directed through the current transformer, the adjustable amplifier/attenuator and the summing circuit to IC201/31 (E/W OUT). The pin cushion control is obtained by adjusting the parabola wave amplitude. The corner correction is also summed to the same parabola wave.

The corner correction, as well as the corner correction balance adjustment value is generated by transforming the vertical ramp square and absolute value to current form and multiplying the values. The result is an adjustment value which is summed to the E/W parabola. The effect intensity can be adjusted with a 7-bit accuracy.

The trapezium correction is generated by amplifying or attenuating the parabola rising or ascending curve part. The effect intensity can be adjusted with an accuracy of 7-bit.

The orthogonal correction is generated by summing a vertical ramp and a parabola wave. The result is used to control the PLL2 phase lock. The correction intensity can be adjusted with an accuracy of 7-bit.

The pin cushion balance is obtained as the orthogonal correction, by affecting the PLL2 function.

The vertical dynamic focus control parabola is generated from the E/W parabola, which is obtained from the point IC201/32. The dynamic focus amplitude is adjustable through the I^2C bus with an accuracy of 8-bit.

4.2.3 Protection functions

To ensure the reliable function of the circuit's external connections and the protection of the picture tube, protection functions have been added to the circuit.

The functions are:

1. The disconnection of the vertical deflection output stage's control signal (H OUTPUT INHIBITATION)

Activated:

- If the supply voltage is under the internal reference of 7.5V
- If the X-RAY voltage is over 8V (IC201/37)
- During the fly-back pulse. This to prevent the vertical deflection output stage transistor from going leading during the fly-back pulse.
- I^2C Drive on/off

2. The disconnection of the vertical deflection control signal (V OUTPUT INHIBITATION)

Activated:

- If the supply voltage is under the internal reference of 7.5V
- During the fly-back pulse
- I^2C Ramp on/off

The circuit contains other protection functions as well. In this version only the previously mentioned are included.

4.3 Function in an operational switching

4.3.1 Supply voltage

The circuit (IC201) supply voltage +12V is brought to pin 18. R222 and C215, 216 function as filtering components. The circuit generates internal reference voltages Vref and Href, which have their own filtering capacitors C226,227 and C205,206. These voltages have a value of approx. 8V. The circuit's actual ground is pin 19. Additionally, the circuit has grounds Hgnd for the horizontal block's and Vgnd for the vertical block's grounding.

4.3.2 Synchronization

The vertical sync pulses are directed from processor (IC501) pin 26 to the deflection driver circuit (IC201) pin 33. Even if the circuit can function independently from the sync pulse polarity, the polarity is standardized positive in the processor. C225 value defines the frequency range of the vertical oscillator. In this monitor model, C225 has been chosen in such a way that the circuit synchronizes automatically to the monitor total frequency range of 50…150Hz. If there are no incoming sync pulses, the vertical deflection is shifted to the free-oscillation frequency of approximately 75Hz.

The horizontal sync pulses are directed from processor (IC501) pin 30 to IC201 pin 38. Also the horizontal sync pulses polarity is standardized positive in the processor. The circuit VCO is tailored so that the circuit synchronizes automatically to the total monitor frequency range of 30…121Khz. The VCO base frequency is defined by C209 and R204. When the processor switches on the largest S-capacitor, more current is summed through R208 to the RC circuit. The addition stabilizes the switching function on lower frequencies.

The frequency feedback is brought from the horizontal deflection output stage to IC201/6 through C210 and R203.

It must be noted that the circuit's composite sync pulse separator switching is unusable, since it cannot generate a sufficiently stable output. The circuit can be run with a composite sync when the field sync pulse separating is done before the circuit, in this case in the processor, and when the phase/frequency

comparator function is prevented during the field sync pulse. The blocking has been accomplished by bringing a field sync pulse at IC201/3 (PLLINH).

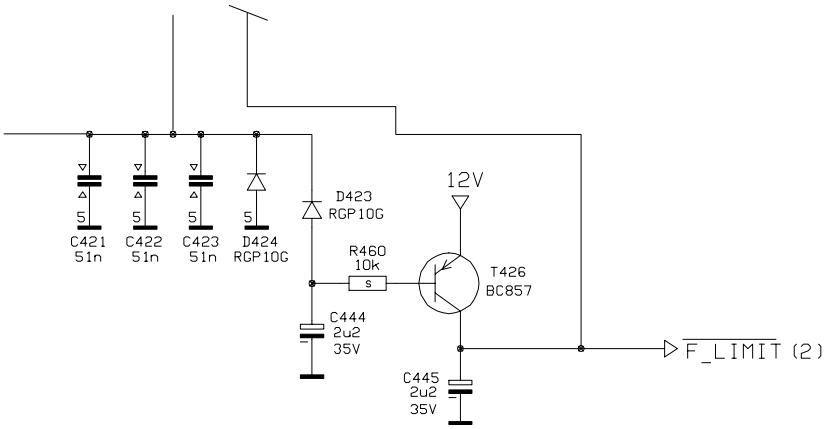
4.3.3 Forced control of maximum /minimum frequency

In order to prevent damaging the horizontal deflection output stage in consequence of an excessively high frequency, the H_Drive signal maximum frequency must be blocked. Since the sync pulses are brought to the deflection driver through the processor, the maximum frequency block is done in the processor.

If the horizontal frequency is excessively high (over 125kHz), its forwarding is prevented by the processor. This prevents, even if the video card would feed an excessively high frequency, the line output stage from being damaged.

Respectively, the H_Drive signal minimum frequency is blocked according the switched S-capacitors. This prevents the monitor horizontal deflection from functioning on excessively small S-capacitors in ratio to the frequency. If the S-capacitors are too small, the AC voltage stored in them grows excessively and the horizontal deflection output stage could be damaged. This situation occurs for instance when changing the monitor mode.

The limiter circuit has been realized in the following way: let's take a hypothetical situation where the horizontal deflection frequency is decreasing thus increasing the AC-voltage in the S-capacitors. When the AC-voltage negative peaks drop under 12V, T426 gets base current through D423 and R460 (F_LIMIT). T426 starts to lead and the voltage in its collector starts to increase. Simultaneously, VCO control voltage tends to increase through D201. At that time, the frequency decrease is halting and the circuit is running on a frequency where the S-capacitor AC voltage negative peaks are approximately 12V. The situation is maintained until additional S-capacitors are switched on. At that point, the AC-voltage in the capacitors is decreasing, T426 goes non-leading and the frequency can decrease to the wanted level.



4.3.4 H-drive output

An H-Drive signal is brought from IC201/21, and is used to control the horizontal deflection output stage transistor T409 through buffer stage T406, 407, 408. The same signal is used to synchronize the width driver IC401. Since IC201/21 output is an open collector type, pull-up resistor R223 is needed.

High voltage data is brought from the high voltage transformer to IC201/15. If the high voltage increases excessively for some reason, [piste] IC201/15 voltage increases over 8V and the circuit ceases to generate the H_Drive signal, at which time the horizontal deflection and high voltage generator are shut down. IC201 will not restart before the monitor has been switched off from the mains switch and restarted.

4.3.5 Phase adjustment

The phase adjustment is realized with phase lock PLL1, which is used to adjust the picture location horizontally. PLL2 compensates the possible heat drifts of the line output stage.

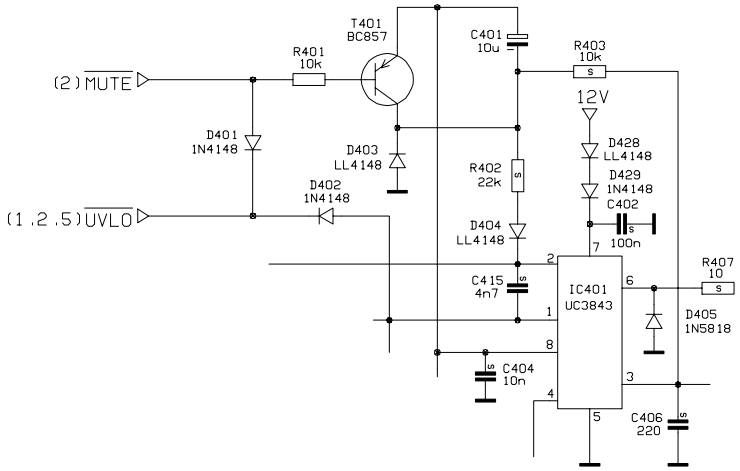
When the user is adjusting the phase, the processor writes a value to the IC201 register, which is converted to DC-voltage (2.8V…4V) by the circuit internal AD-converter. This DC-voltage defines the area of the VCO saw tooth wave (measurable at IC201/10) where PLL1 should compare line sync pulses. When the DC-voltage is altered, the compared area is also altered, at which point the saw tooth wave and the H_Drive signal move to a different location in relation to the sync pulse. The user can see this on the monitor screen as picture motion to the left or right depending on the adjustment direction.

4.3.6 Frequency change behaviour

When the monitor deflection frequencies are altered (mode change), the monitor screen must be blanked. The mode change seems more fluent when there are no vague flashes on the screen. On the other hand, the horizontal deflection output stage reliability can be increased if the picture width is narrowed before the mode change. The screen blanking must be rapid, but at the same time long enough to let the new mode settle before returning the picture.

Data about a possible phase lock clamp to the incoming sync pulses is brought from IC201/37. When a frequency change occurs, IC201/37 goes up, at which time T203 starts to lead. As a result, T205 connects C245 positive end to ground. G1-grid goes negative, thus blanking the screen. When changing modes, also IC501/11 goes up and disconnects the video signal in the video amplifier.

The forced narrowing in mode change situations is realized with the MUTE line. When the frequency is altering, deflection driver IC201 pin 37 goes up, at which point the MUTE line goes down. The MUTE-line pulls T401 leading through R401, at which time IC401/8 (Vref) connects to the width control voltage and through R403 to the current sense input (pin 3). As a result, the pulse ratio is decreasing and the picture is narrowed. The situation is slowly restored, since after T401 has shut down, there is still current flowing through C401 to IC401 pin 2. The picture width is restored only after the full reload of C401.



4.3.7 Vertical deflection control

Vertical deflection is used to adjust the following parameters:

Picture height is controlled by altering the vertical ramp amplitude. In the procedure, the processor writes a value to the IC201 register, which defines the circuit's internal amplifier amplification. As the ramp amplitude is increasing, the current in the deflection coil is also increasing, thereby increasing the picture height.

The vertical ramp is brought from IC201/29 and directed through R271 to IC203/1 inverted input.

Vertical centering is realized by connecting DC-voltage to the vertical output stage IC203 positive input. The voltage is generated with the IC201 internal D/A converter. The transform value has been written to IC201 memory by the processor through the I^2C bus. The adjustment value fluctuation interval is 3.2…3.8V. The DC-level has been optimized with R270 and R272. When the IC203/28 (VDCout) output voltage differentiates from pin 29 (Vout) permanent 3.5V DC-voltage, the DC-voltage levels from the vertical output stage (IC203) inputs (pins 1 and 7) are unequal, thereby generating a DC-current component to the vertical output stage control. At that point, DC-current is flowing from the output stage to the deflection coil, or vice-versa. As a result, the picture location shifts vertically.

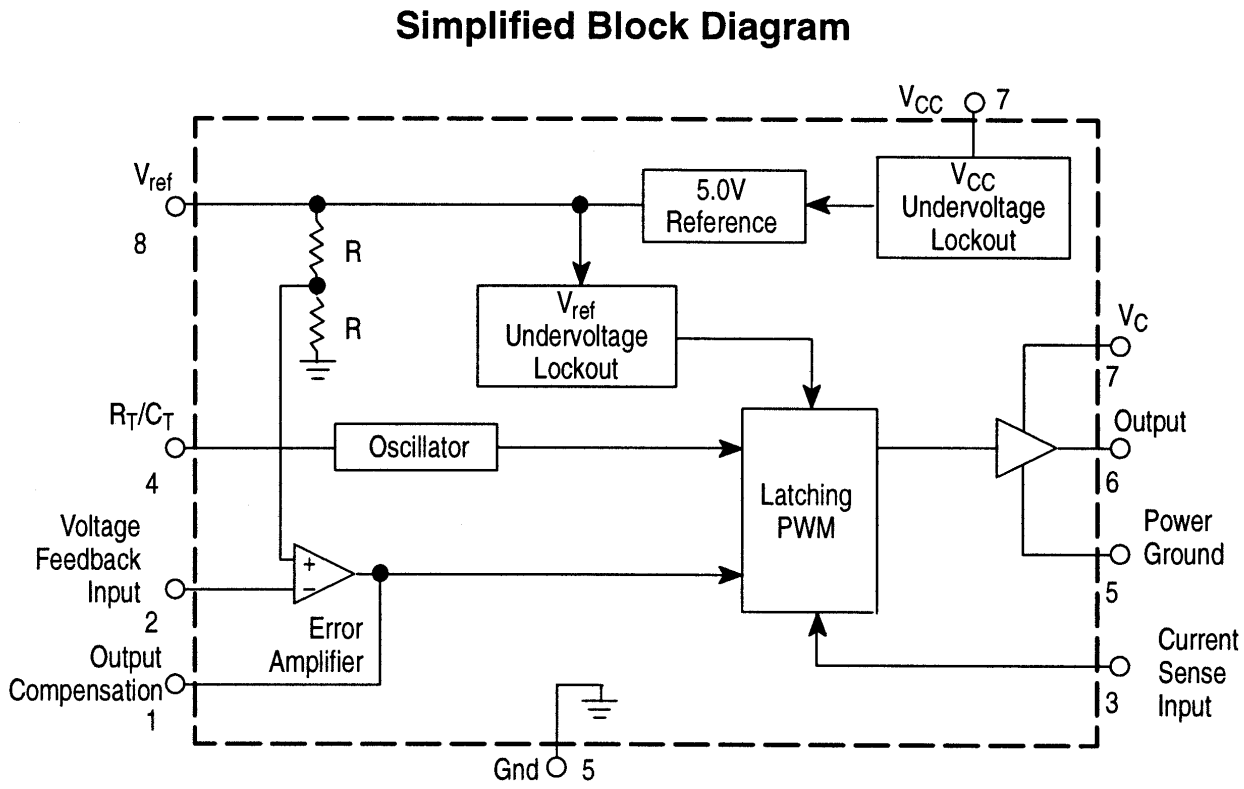
When adjusting vertical centering, the geometry correction voltages amplitude must be altered, otherwise the vertical lines will not stay straight when shifting the picture vertically. The needed correction is realized by connecting internally the DC-voltage data (VDCout) to the geometry signals generator block.

5. Width control circuit

5.1 General features

The width control circuit is formed by current form pulse width modulator UC3843 (IC401), switch mode FET T403 and switch mode transformer M401. The transformer contains a primary coil and two secondary coils (one fly-back-type and one forward-type). The supply voltage is fed from the fly-back coil to the line output stage, and the needed power to control T405 is brought from the forward coil. The forward-switching in the T405 control enables the needed base voltage increase when the line frequency is rising. The pulse width modulator is synchronized to line frequency with the H_DRIVE signal.

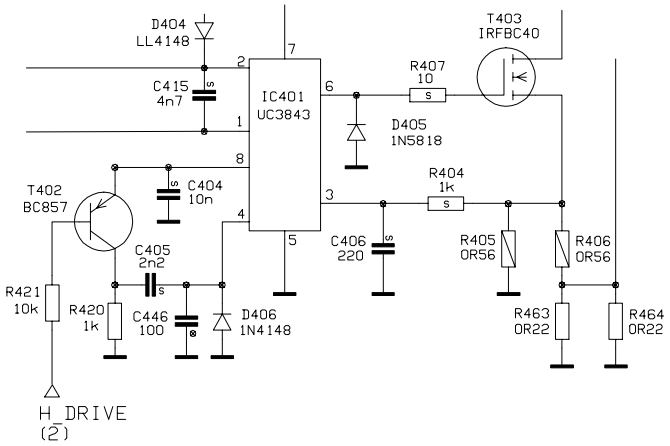
The UC3843 block diagram is illustrated in picture 4.



picture 4

5.2 Function

The pulse width modulator is triggered from the H_DRIVE pulse through T402. T402 starts to lead with a falling edge and connects a +5V from IC401/8 (Vref) to RC-circuit R420 and C446, at which point the decision level is reached, and the circuit is triggered. As a result, IC401/6 goes up, T403 goes leading and current starts to flow in the primary coil of transformer M401. When the voltage in current sense resistor R405 is increasing to the same level as in the current sense comparator's negative input, the RS-flip-flop controlling the circuit output stage is reset, and the output (IC401/6) goes down. The energy transferred into the secondary starts to charge the S-capacitors through D410 and D430. Simultaneously, C414 is charging through D411 and L402. The procedure is restarted in the next falling H_DRIVE pulse edge.



5.3 Width control, E/W and trapezium correction

The picture width is adjusted with the voltage amount coming to the differential amplifier (WIDTH). The voltage is generated with the PWM output (DA7) of processor IC501. The voltage filtering components are R514/559 and C509/529.

Due to the nature of the IC401 internal differential amplifier, it tries to hold the IC401/2 voltage at a constant 2.5V level, which means that when the picture is widened, the control voltage from the processor is decreasing. At that time, the differential amplifier output voltage starts to increase (pin 1), resulting to the increase of the current sense comparator negative input and primary switch of current. More energy is stored to the secondary.

The feedback voltage data is generated from a fly-back pulse, which level is first decreased with capacitor divider C416, C418 and rectified with D408.

Due to the higher supply voltage of the line output stage, the fly-back pulse height is also higher. The secondary voltage alteration increases IC401/2 (Vfb) voltage until it reaches the 2.5V level. At that point, the picture width is at the wanted level and the adjustment has stabilized.

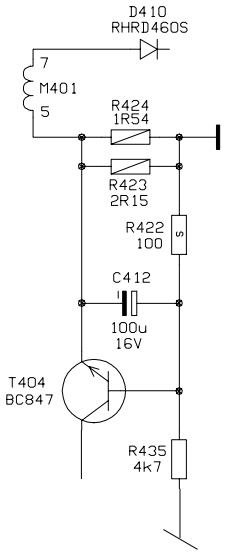
A feedback circuit has been brought back to the input from the differential amplifier output through R408 and C403. The circuit's purpose is to filter disturbing voltages from the differential amplifier output and to limit the upper frequencies amplification to prevent oscillation. Trimmer RT401 is used to set the picture width roughly to the correct area.

The E/W and trapezium correction are done by summing the E/W-parabola and trapezium correction voltages to the width control voltage with R409.

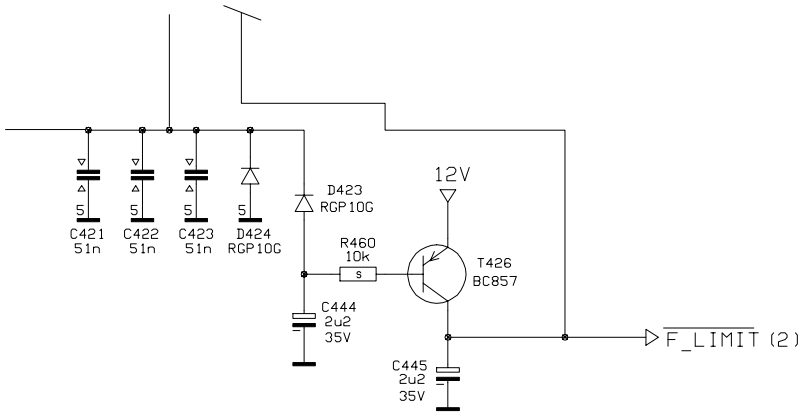
5.4 Current block

The current used by the line output stage flows through R423 and R424. If the line output stage current increases excessively, transistor T404 emitter voltage decreases enough to start T404 leading. As a result, T404 collector and IC401/1 (comp) voltage is decreasing.

IC401/1 is the differential amplifier output which controls the reference level of the current sense comparator. When the reference voltage is decreasing, T403 control is disconnected even with a low primary current, and no excessive power is transferred to the secondary. If the shortcut has not been resolved during the next line, the procedure is repeated.



T404 can be driven leading also through T426 and R435. In a situation where T409 has been damaged, thus pulling the line output stage supply voltage to the ground, T426 base is connecting to ground through R460 and D423, and T426 starts to lead. As a result, T404 opens and pulls IC401/1 to ground, at which point the pulse ratio and secondary voltages are decreasing.



T425 is used to control a possible situation where the width switch mode is starting up, but the line output stage not. In this situation, the DC-voltage of the S-capacitors increases to a dangerous level. R414 and R413 form a voltage divider, and when R413 voltage loss increases enough, T425 connects more power from the 190V voltage to the feedback voltage data, resulting to the decrease of the pulse ratio and secondary voltages.

These circuits protect the power supply and other circuits in a line output stage failure situation.

When repairing line output stage failures, the component causing the damage of some part must be found before installing a new part. It is very unlikely that a discreet component would be damaged without a cause. The current limitation components and function must be checked in every failure situation.

6. High voltage generator

6.1 General

The high voltage is generated by high voltage transformer M301, and a fly-back type voltage regulated power supply composed of transistors T304, T303 and IC301. In addition to primary- and secondary coils and secondary diodes, the high voltage transformer contains a Bleeder-resistor, trimmers for the focus- and G2-voltage adjusting, and a high voltage capacitor. Also an OVER VOLT-voltage is brought from the transformer's auxiliary coil (M301 pin 2). The voltage is used to monitor the excessive increase of the high voltage in a possible failure situation. The feedback data for the high voltage regulation is brought from the Bleeder-resistor lower end (M301, pin 16) with the voltage forming into resistors R323, R322 and RT301. Trimmer RT301 is used to adjust the high voltage to 27kV.

6.2 The function

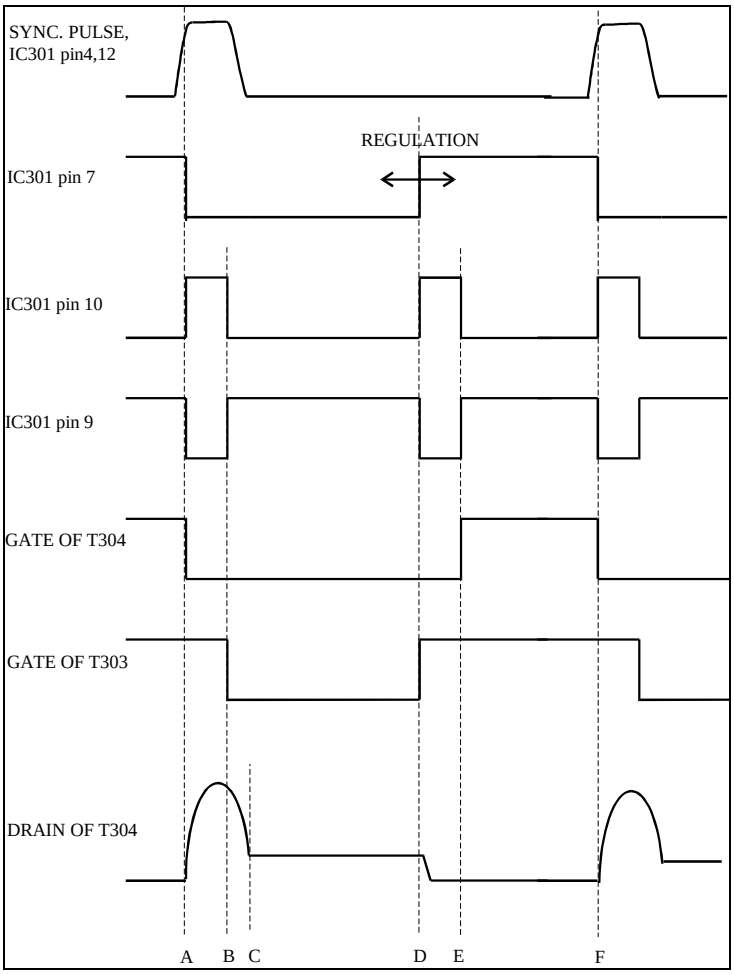
Refer to picture 5

The high voltage generator function can be compared to the monitor power supply, since the function principle is very similar (fly-back power supply) and common switching elements can be found in the circuit. A 190V DC-voltage is present at the higher end of the primary coil (pins 9 and 10), and switch mode switch T304 can be found on the lower end. When T304 is leading, current flows through the primary coil, at which time energy is stored to the high voltage generator, just like with the power supply. When T304 is directed non-leading (section A), a fly-back pulse is generated to the T304 drain (time period A…C in the picture). The high voltage generator's secondary diodes start to lead and the energy stored in the primary is transferred to the capacitance in the high voltage generator and the picture tube.

Since the coupling factor between the high voltage generator primary and secondary is very small (unlike in the power supply transformer), the switch mode switch's drain voltage is not disconnected as in the power supply, but ringing is easily generated on the drain. Capacitor C307 has been added to the drain to limit the maximum voltage and frequency of the drain oscillations.

As distinct from the power supply, T304 drain has a large capacitor (C307), and this capacitor must be discharged before switch mode switch T304 is again made leading. Otherwise the capacitor would discharge through the switch mode switch and the switch would overheat. On the other hand, the drain oscillations must be removed after the fly-back pulse, in order to the voltage regulation to function properly. This has been realized with switch T303. Just before the fly-back pulse end (moment B), switch T303 is directed leading. At that time, after the fly-back pulse, the current flowing in the primary coil from pin 10 to pin 9 is going to a loop: primary coil - T303 - D306. This phenomenon starts at the moment where capacitor C307 has been discharged to just under 190V, and diode D306 is turning to forward direction (moment C). The phenomenon is active as long as T303 is leading and T304 non-leading (time period C…D). Just before T304 is redirected leading, T303 is directed non-leading (moment D). At that time, the current in the primary coil is forced to flow: primary coil - 190V capacitors (C140,141) - C307, and the latter starts to discharge.

When C307 has been completely discharged, the current flows instead of C307 through a T304 diode, not illustrated in the block diagram (time period D…E). At this point, T304 can be made leading (moment E). Since the voltage over the primary coil is now over 190V, the primary coil current turns rapidly to flow from pin 9 to pin 10 and further through T304 to the ground; energy is stored to the coil etc. and the sequence is restarted.



picture 5

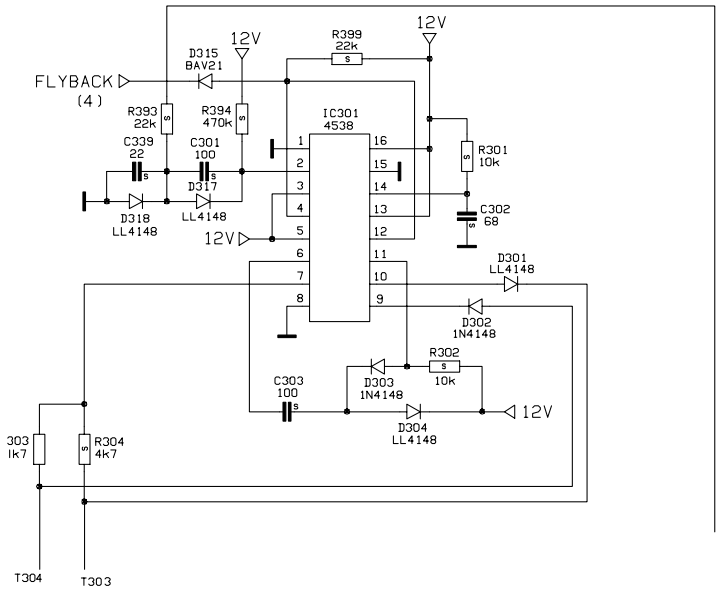
6.3 HT-driver

The correctly timed control of the switching transistors is accomplished with monostabile flip-flop IC301, which is realized with 4538. The circuit contains two identical monostabile flip-flops, whose time constants are defined with external components.

The incoming sync pulse rising edge triggers both monostabiles A and B (A = pins 1 to 7 and B = pins 9 to 15) at moment A. At that point, monostabile A pin 7 (inverted output) goes down and pulls down T304 grid with T306. T304 goes non-leading, and the high voltage fly-back pulse is started.

T303 is still non-leading. After a time constant defined by R301, C302, monostabile B shifts its mode and its output pin 10 goes down. The time constant is time period A…B in picture 5. Since pin 7 voltage is down, T303 grid is goes down with R304 and T302, and T303 goes leading.

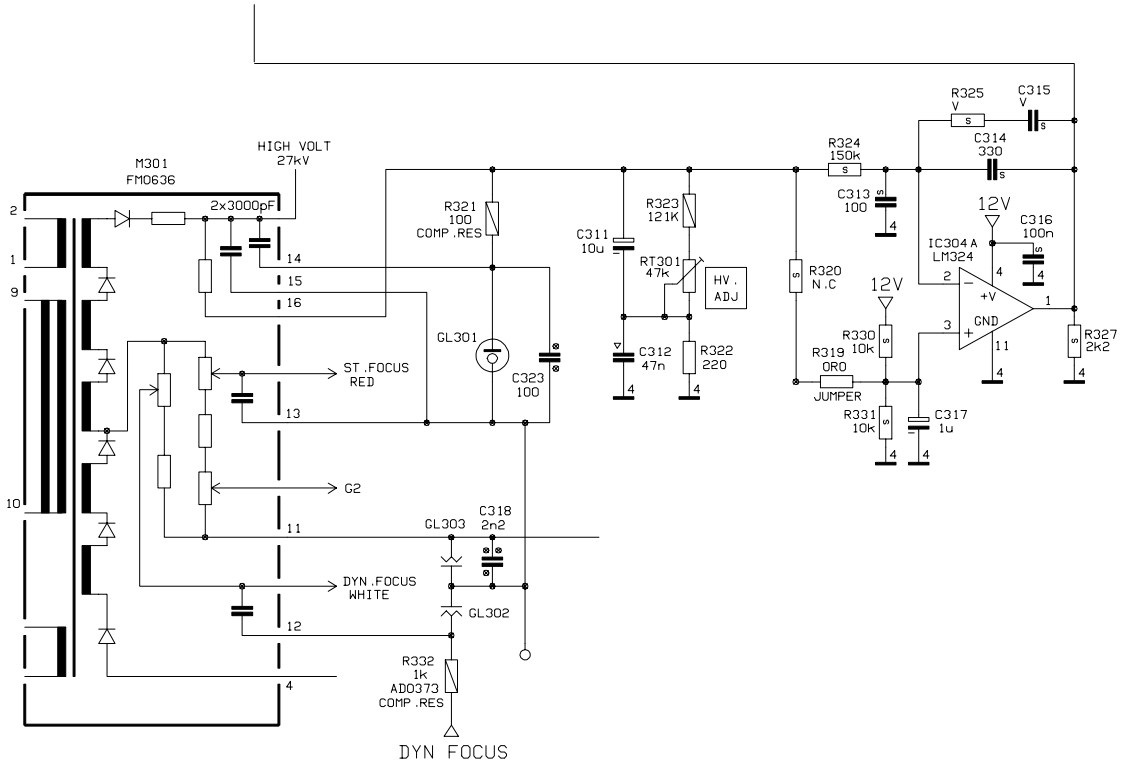
At the moment defined by the high voltage regulation, monostabile A reaches its decision level (moment D in the picture), output pin 7 goes up and respectively inverted output pin 6 goes down. T303 grid goes up with R304 and T301, and T303 is directed non-leading. The change in pin 6 triggers monostabile B, which shifts its mode. Pin 9 goes down, thereby preventing T304 grid from going up through R303. After a time constant defined by R301 and C302 (moment E in the picture), monostabile B pulse is ended and pin 9 goes up. T304 grid can now go up, and T304 is directed leading. At that time, energy is stored in the high voltage transformer's primary coil. At moment F, a new trigger pulse is arriving, T304 goes non-leading, the fly-back pulse is started. The energy stored in the primary is transferred to the primary etc.



6.4 Regulation

Unlike in the power supply (current shaped regulation), the high voltage stage regulation is voltage shaped, that is, the pulse ratio of the switch mode switch is altered with the feedback data given by the secondary. The longer the switch mode switch T304 leading time, the higher the primary current and the larger the energy amount transferred to the secondary, thereby enabling a higher load to the secondary.

Here is an example: if the beam current increases, the high voltage tends to decrease. Due to this, the C311 voltage located at the lower end of the Bleeder-resistor tends to decrease. As a result, also the high voltage differential amplifier IC304/2 voltage tends to decrease. IC304/6 is the reference voltage (approx. 6V) where the high voltage feedback is compared. As a result, IC304 pin 1 voltage increases, at which point monostabile's capacitor C301 charging time is decreased. In the previously illustrated picture, this means that moment D shifts to the left, thereby decreasing the time T304 grid is down, thus decreasing the time T304 is non-leading. As a result, when T304 grid goes up at moment E and T304 starts to lead, its leading time is increased before the new triggering pulse at moment F. Trigger pulses are in line frequency, thereby rendering time period A - F constant. Since T304 leading time is increased, more energy is stored in the high voltage transformer's primary coil, at which point T304 goes non-leading again, more energy is stored in the secondary coil, and the high voltage increases back to the wanted level.

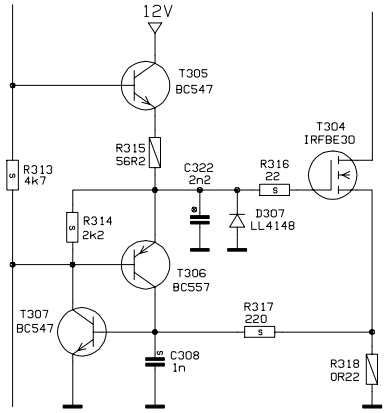


6.5 Current limiter

The high voltage generator's current limiter is realized with T307 and T306. The current limiting protects the generator for instance in the start-up situation, when the generator tends to give as much current as possible to the secondary. The current limiter is also needed in possible failure situations.

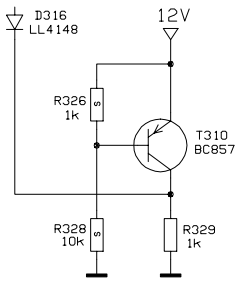
If the high voltage generator current increases excessively, current sense R318 voltage increases to a level where T307 and furthermore T306 start to lead. This keeps T307 leading, so the circuit functions like a thyristor. Since transistor T304 grid connects to the ground due to the transistors' leading, the current flowing through the high voltage transformer primary coil is also disconnected. T307 and T306 keep leading as long as T305 is leading. When the control from IC301 to T305 is disconnected, T307 and T306 go non-leading as well, since the needed control hold current is disconnected. When IC301 gives the next pulse to T304, the function is repeated if the over current situation has not been resolved.

When repairing high voltage stage failures, the current limiter components and function must always be checked.



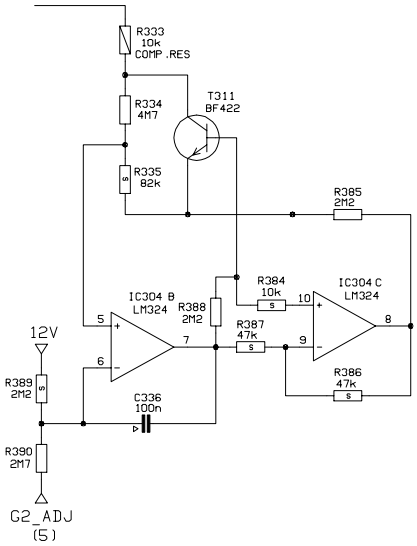
6.6 Start-up sequence

To ensure the proper function of the start-up sequence , the high voltage stage function is prevented when IC301 supply voltage is too low. This is realized with T310. When the 12V voltage is low, T306 base is connected to the ground through D316 and R329. At that time, if T305 is leading, T306 is leading as well and high voltage switch T304 grid stays down, preventing it from conducting. This prevents possible failure situations from damaging the high voltage stage in a start-up situation. When the supply voltages have increased to the proper level, T310 connects leading and +12V is connected to the D316 cathode. After this procedure, the high voltage stage can normally start up.



6.7 G2-voltage generating stage

The G2-voltage is controlled with a circuit composed of T311 and IC304. The principle of the adjustment is to alter the Focus-adjustment unit lower end voltage, thereby altering simultaneously the G2-voltage from the trimmer. If a G2-voltage increase is needed, the processor increases the G2_ADJ-voltage (max 5V). Simultaneously is the IC304/6 pin voltage increasing which causes the decrease of the output voltage (pin 7). When T311 control is decreasing, the focus-unit lower end voltage is defined by resistor chain R334 and R335, thus increasing the G2-line voltage. Correspondingly, if the G2_ADJ voltage is decreasing, T311 control is increasing and the voltage in the G2-line decreasing.



6.8 X-ray protection

A pulse proportional to the high voltage is brought from high voltage transformer M302 pin 2, used to prevent the generating of x-ray radiation in a failure situation, where the high voltage tends to increase excessively. The pulse is transformed to DC-voltage with D305 and C304. This voltage is connected with R306, R307 and R308, decreased to a proper level, to deflection driver IC201 X-ray-in pin 15. If this pin voltage increases over 8,0V, the circuit interrupts the Driver pulse feed to the line output stage. Since the high voltage generator gets its trigger pulse with a line fly-back pulse from the line output stage, the high voltage generator is also shut down. This prevents the high voltage from increasing excessively. Since the deflection driver feeds a new driver-pulse only when its supply voltage has dropped, the monitor must be shut down for a moment.

7. Vertical output stage

Vertical amplifier IC203 is of type STV9379, and operates in theory like an operational amplifier. The supply voltages are fed to the circuit: 15V to pin 2 and -13V to pin 4. A vertical ramp is brought from deflection driver IC201/29 (Vout) through R271 to the IC203/1 inverting input, and a voltage reference (VDCout, IC201/28) through R270 to IC203/7 non-inverting input. The VDCout voltage level is used to define the picture's vertical centering. Output voltage IC203/5 is fed to the deflection coil. R278 and R279 are used to generate a voltage proportional to the deflection current, which is connected through R277 and C234 to IC203/1 inverting input, thereby defining the circuit's amplification. Attenuation circuit R280, R281 and C233 is used to attenuate the oscillations generated during the vertical fly-back, which could appear in the picture upper edge as linearity default or fly-back lines. C234 is used to prevent circuit oscillation on high frequencies. D207 is the diode needed by the fly-back pulse generator, used to sufficiently increase the fly-back pulse and thus decrease the fly-back time. A positive vertical fly-back pulse is brought from IC203/3, with an amplitude of approx. 27V. During the sweep, the voltage of the pin in question is approx. -11V and during the fly-back approx. 16V. The protection circuit inside the vertical output stage protects the circuit in short-circuit situations and from overheating.

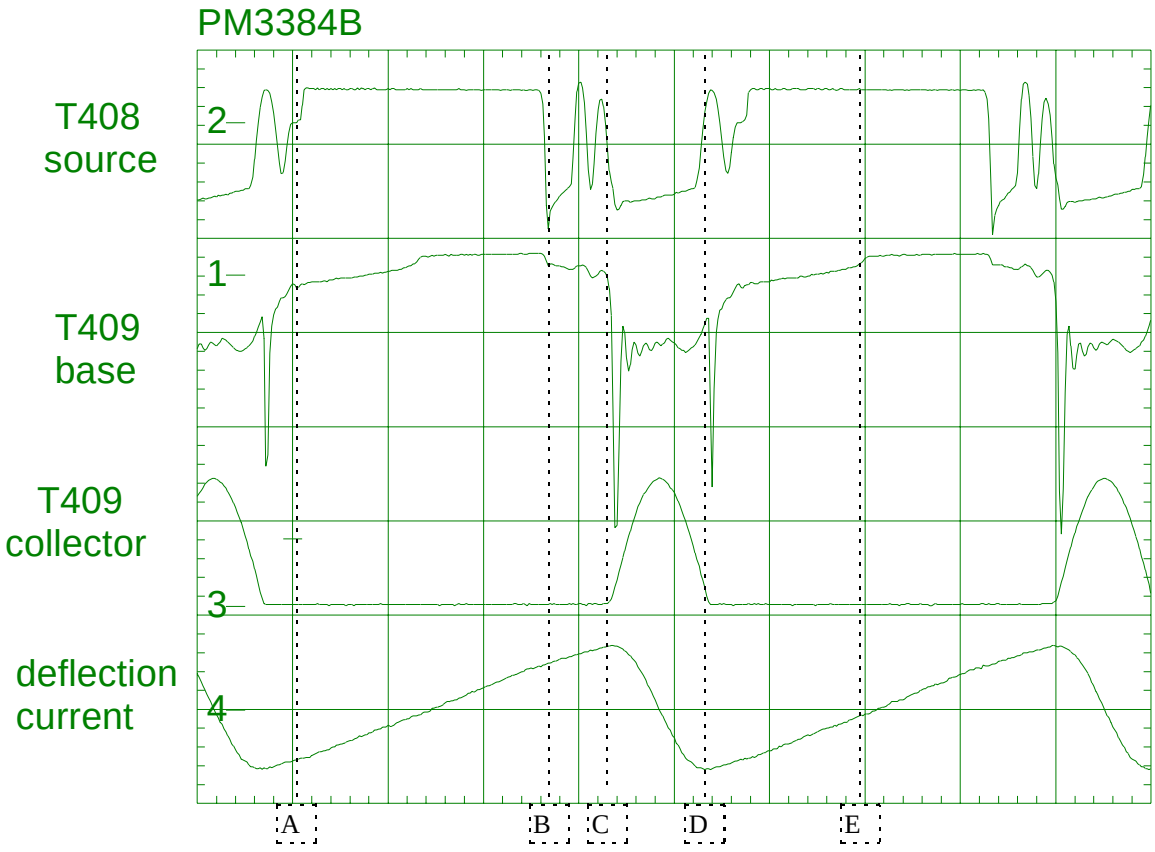
8. The line output stage

8.1 General

The line output stage is composed of output transistor T409, fly-back diode D414, fly-back capacitors C416 and C418, as well as driver FET T408, and its buffer circuit T406, 407, and driver transformer M402. Also included are the S- and linearity-correction circuits, the frame centering circuit and the current limiter circuit.

8.2 The function

The function is illustrated in picture 6



picture 6

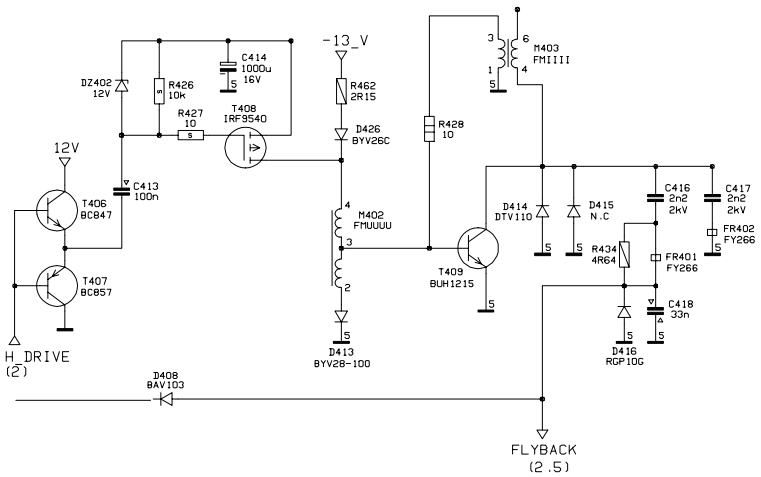
The line output stage gets its first positive Driver-pulse (amplitude approx. 10V, **falling** edge) from deflection driver IC201/21, section A in the picture. This pulse gets driver transistor T408 to lead, thereby causing current to flow in the driver transformer coils. T409 base voltage starts to increase, and as a result T409 starts to lead. Due to the coil's winding direction and coupling ratio, M402 pin 2 voltage is negative, at which point D413 is not leading. Current starts to flow from the S-capacitors through the deflection coil to T409. The current increase rate is relative to the deflection coil's inductance and the S-capacitors voltage amount. The electron beam moves from the picture center toward the right edge and energy is simultaneously charged to the deflection coil. When the Driver pulse is decreasing (section B), M402 pin 3 has an approx. 0.5V voltage as a result from T409 base charge. When pin 4 voltage has dropped and pin 3 has a positive voltage, pin 2 voltage increases, thereby causing D413 to conduct and discharge T409 base charge. When the discharging has been done, the transistor shuts down rapidly (section C). The electron beam is in its utmost position on the right.

Since there is energy in the deflection coil and T409 is not leading, the oscillation circuit composed of the deflection coil and fly-back capacitor C416, C417 (and C418, in serial with C416) starts to oscillate. As a result, the deflection coil energy is transferred to fly-back capacitor (period C-D). At that time, the fly-back capacitor voltage increases to a very high level of approx. 1200V (line fly-back pulse, FBP). Simultaneously, the horizontal deflection direction in the picture tube is reversed and the electron beam (which is blanked, and not visible on the picture surface) starts to move rapidly from right to left.

When the total amount of energy has been re-transferred from the fly-back capacitor to the deflection coil, the deflection current is in its negative maximum, and the electron beam in its utmost position on the left (section D). At that time, the oscillation circuit composed of the deflection coil and the fly-back capacitor tries to continue its oscillation during the negative half period, but fly-back diode D414 prevents this. Since there is still energy in the deflection coil (which cannot disappear by itself), deflection current starts to flow from the deflection coil through S-capacitors to the ground, and further through the fly-back diode back to the deflection coil (period D-E). At that time, the electron beam deflects toward the picture tube center. When the energy in the deflection coil is zero, the beam is in the screen center (section E). Before this moment, Driver transistor T408 has gone leading with the decreased driver pulse (section D). At that point, when the deflection current is zero, T407 starts to lead and the sequence starts from the beginning (section D).

T409 does not start to lead at moment D, since current is flowing through the fly-back diode, at which point the transistor collector is negative in relation to the emitter.

Capacitor C418 is used to generate the approx. 70V fly-back pulse needed in the horizontal blanking. D416 is the level [clamp] diode, which is used to clamp the voltage to the ground during C418 sweep.



8.3 Linearity correction

Since this monitor operates in a large frequency range, frequency relational S- and linearity-correction is needed in the horizontal deflection. For this purpose, the line output stage contains electrically switched S-capacitors C429-C435, their switching FETs T418-T424, and linearity coils L403, L404. The linearity coil's inductance can be altered with parallel coils L405/L406, which are controlled by switching FETs T413 and T414.

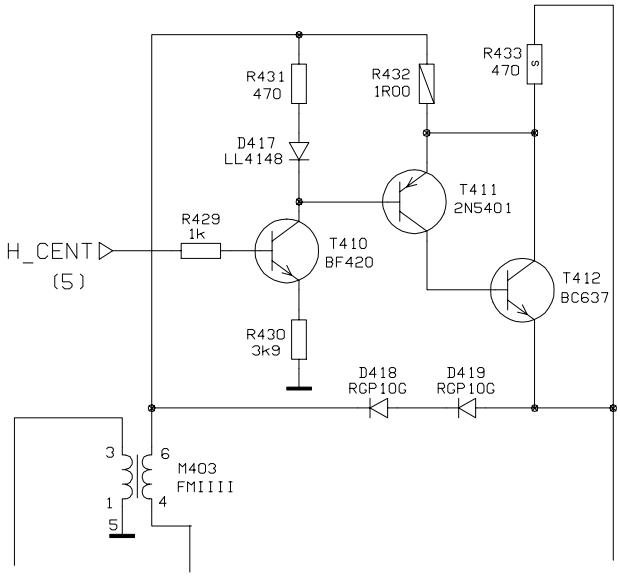
The processor selects the appropriate combination from the S-capacitor table according the used horizontal deflection frequency, and directs the corresponding switching FETs leading through lines S0…S6. The principle is: the lower the line frequency, the more capacitors are switched.

The linearity correction is accomplished with linearity coils L403 and L404. Since the coils correction effect is excessive with high frequencies, only both or just one of the parallel coils are connected parallel with the linearity coils. This is accomplished by the processor, which pulls down the wanted pin (LIN 1 or LIN2). R436 and D420 remove oscillations occurring in the linearity coil.

8.4 Frame centering

The frame centering is accomplished with transformer M403. When the current needed by the line output stage is fed to the S-capacitors, DC-current is simultaneously flowing through the deflection coil to T409. When the current is flowing through the deflection coil, it causes frame deviation to the right. Due to this, as well as the tube/deflection coil tolerances, the frame centering need is greater to the left than to the right. Centering transformer M403 is connected parallel with the deflection coil. DC-current can be generated to its coil 6…4 if the impedance affecting the current is different when flowing from pin 6 to pin 4, than when flowing from pin 4 to pin 6.

When the processor directs H_CENT line down, transistor circuit T411, 412 is completely non-leading, and current can flow only to the other direction through D418 and D419. The transformer's DC-current is now at its maximum, and it nullifies also the DC-current going through the deflection coil, thus shifting the frame to the left. If the H_CENT line voltage is increased, also transistors T411, T412 start to lead gradually. Current can now flow to the other direction as well, at which time the DC-current through the transformer is decreasing, and the frame is shifting to the right. When the H_CENT line voltage is 5V, T411 and T412 are completely leading, and the current through them is slightly higher than diodes D418, D419, at which time the frame has shifted to its utmost position on the right.



9. Blanking circuit

Line and field fly-back blanking is accomplished through G1 grid. The grid control switching is composed of T205…T208, C246, R236 and R229. When both blankings are inactive, DZ201 regulates through T206 an approx. 20V voltage to C246.

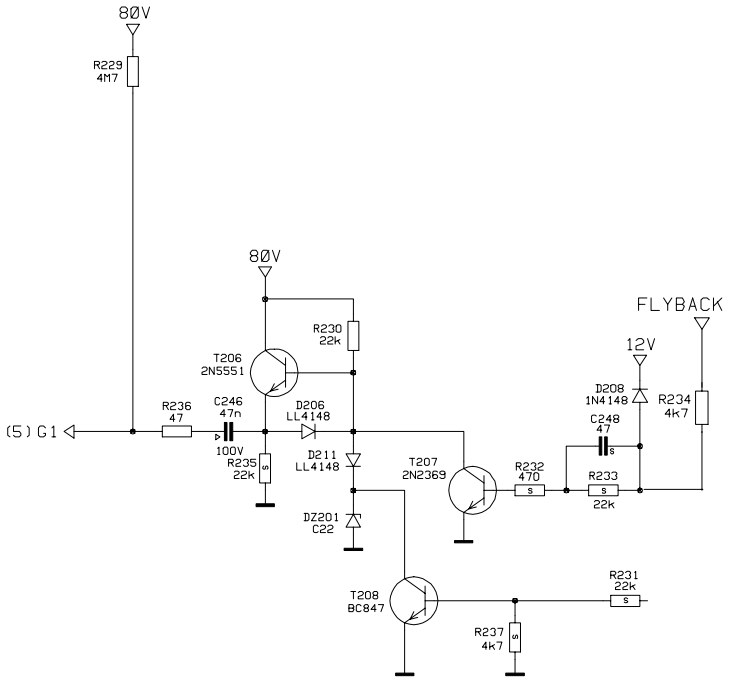
Line blanking

A FLYBACK signal brought from the line output stage is used in the line blanking. The signal connects T207 leading through R232/233. As a result, C246 positive side connects through D206 to ground, at which point a negative 20V pulse is generated to the G1-line, thus causing the beam blanking.

R233 is parallel with C248, used to override R233 with the FLYBACK pulse's leading edge, resulting to an increased base current to T207, and a faster move to conduct. When T207 is leading, T206 base voltage drops so low that C246 is not loaded from the 80V power during the blanking.

Vertical blanking

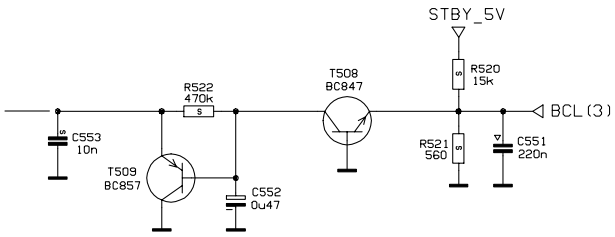
A vertical fly-back pulse from IC203 is used in the vertical blanking, which connects T208 leading through R231/237. As a result, C246 positive end connects through D206/211 to the ground, and a negative blanking pulse is generated to the G1-line. Part of the vertical sync pulse is summed through D209 to the vertical fly-back pulse. This prevents a short fly-back line from generating on to the picture lower edge.



10. Other functions

10.1 Beam current limiter circuit

The beam current limiter circuit is composed of T508 and T509. The beam current flows from ground through R521 to high voltage transformer M301 pin 4 (secondary lower end). When the beam current increases excessively, T508 starts to lead. At that point, also T509 is leading, and thereby decreases the contrast adjustment voltages. As a result, the beam current decreases. C551 prevents short beam current alterations from affecting the beam current limiter. R522 and C552 long time constant prevents the brightness alteration “pumping” when the beam current of successive pictures is different.



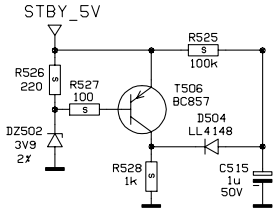
10.2 TCO-compensating circuit

The compensating circuit’s purpose is to prevent the progress of a forward directed magnetic field generated by the deflection coil. The compensating is accomplished with a wire loop located on the picture tube’s upper edge. The loop current is brought from the horizontal deflection current generated by the line output stage, and when flowing in the wire loop, the current generates an opposite directed magnetic field which overrides the deflection coil field. The compensating must be accomplished in order for the monitor to meet the TCO-standard radiation requirements.

10.3 Reset-circuit

The reset circuit is composed of T506, DZ502, and their auxiliary components. When the monitor is switched on, STBY_5V voltage increases and charges R525 through C515. When the voltage has increased over the RESET-pin decision level, the processor is switched from reset-mode to normal-mode.

When the STBY_5V voltage reaches the nominal value, T506 is also leading, and D504 cathode has 5V. If the STBY_5V drops under 4.5V, T506 is switched off and C515 starts to discharge very rapidly through R528, at which point the processor gets a reset and moves to defined routines.

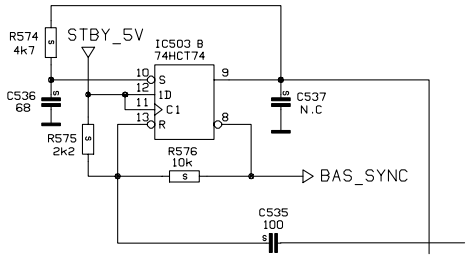


10.4 Clamp pulse generating

The black level clamp pulse needed by the video is generated with a horizontal sync pulse. Since the monitor operates also with a sync on green-synchronization, the clamp pulse's place and length must be precisely defined. The circuit is composed of IC503, R574/575, and C535/536.

Since IC503/12 (D) pin is connected directly to STBY_5V, the circuit output (pin 9) is automatically up, and pin 8 down. R575 and R576 form a voltage division, used to generate the 4V DC-voltage. When the H_SYNC pulse is connected through C535 to IC503/15 (R), the point's voltage is increasing on the pulse rising edge, when C535 is simultaneously charging. When the H_SYNC pulse falling edge pulls C535 positive end to the ground, IC503/13 (R) negative pulse is generated and the circuit output changes its mode.

As a result from the mode change, C536 start to discharge through R574. When IC503/10(S) voltage has dropped under the circuit's decision level, the output is set to start-up mode at 5V. The circuit triggering is accomplished with the H_SYNC pulse's falling edge, at which point the black level clamping hits the appropriate location (back porch) also with a "sync on green" synchronization. A pulse line can thereby be generated from the H_SYNC signal, with a negative pulse length (approx. 500ns) and a constant location. The sequence is restarted with the next H_SYNC pulse.

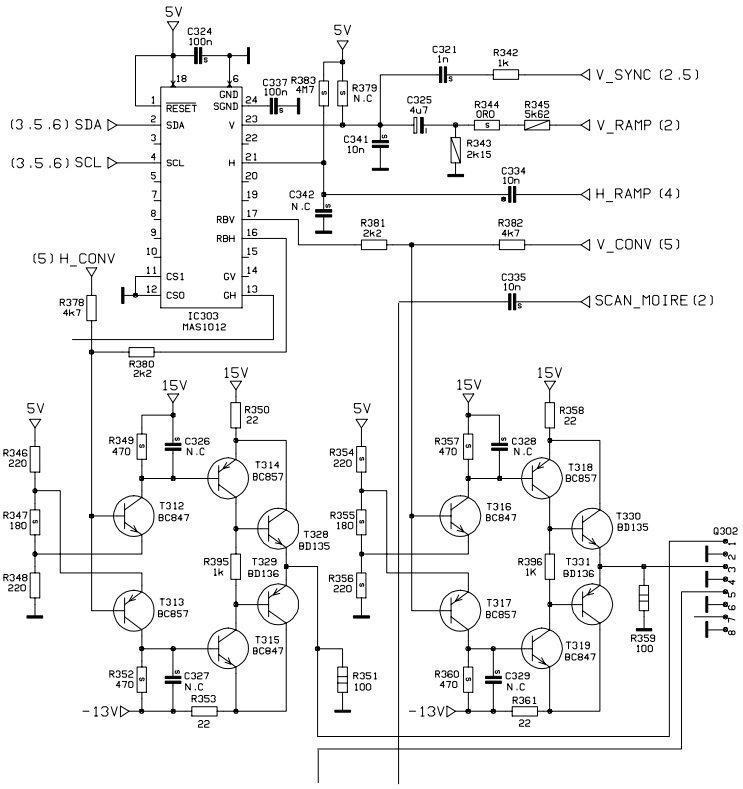


10.5 Dynamic convergence

In a 21" high end monitor, a convergence adjustment (static convergence) affecting the whole picture field is not sufficient. The picture field is divided in 25 parts (5x5 grid). Every part's red/blue convergence is separately adjustable both vertically and horizontally (dynamic convergence). The required ferrite core coils are installed to the picture tube neck, which can be controlled to adjust the dynamic and partly also the static convergence.

IC303 gets the adjustment value table from IC501 through the I^2C bus. The line frequency ramp wave is brought from IC303/21 and the field frequency ramp wave from IC303/23. IC303 recognizes from the ramp waves in which matrix grid the sweep is taking place, and generates the corresponding adjustment values to the output pins. The adjustment voltages for the buffer output stages are starting from IC303/16 (blue-red horizontal direction) and IC303/17 (blue-red vertical direction). The adjustment's mid position is a 2.5V output voltage. The effect increases toward zero and 5V so that when the adjustment voltage is over 2.5V, the +15V voltage output transistors (T330 and T328) are leading, and when under 2.5V, the -13V voltage output transistors (T329 and T331) are leading. The picture field output voltages do not change abruptly, but slide from one adjustment value to the other. In fly-back periods the changes can be rapid.

The static convergence is adjusted with permanent magnets during the picture tube manufacturing. In this monitor, the static blue/red convergence can be adjusted electrically as well. DC-voltages H_CONV and V_CONV brought from IC501 pins 46 and 47 are summed to the dynamic convergence adjustment voltages.

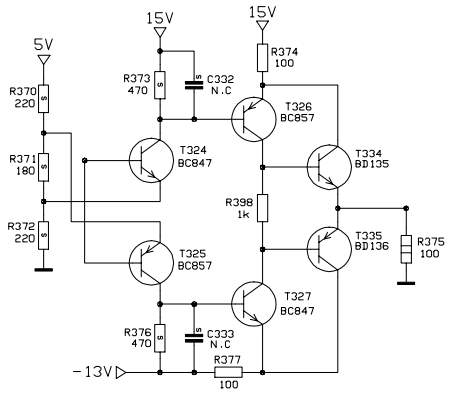


10.6 Moiré adjustment

Moiré can appear as VIDEO- or SCAN-Moiré. The principle in this correction circuit is to correct both Moiré phenomenons simultaneously. The Moiré-control is generated with line driver IC201/2. The circuit outputs rectangular wave, with a frequency half the line frequency. The rectangular wave phase is altered after each field (vertical deflection sequence). The wave amplitude (0…2V) can be adjusted with a 5 bit accuracy through the I^2C bus.

The **video-moiré** effect is decreased by changing the PLL2 phase lock function. R201 is used to connect voltage with a ratio defined by voltage division R201/202 from the rectangular wave to filter capacitor C202's lower end, at which point the line phase is altered. When the shift is accomplished with every other line, a vertical saw tooth wave is generated from the starting points. At the next field, the rectangular wave phase has been altered 180°, the saw tooth waving is compensated and the vertical line is straight. Video-moiré generating can be decreased by using this procedure.

Scan moiré is decreased by altering the line position vertically. The shift is accomplished with a coil installed in the picture tube neck. Power is fed to the coil with an amplifier switching formed of T324/327 and T334/335. Since the stage is AC-connected with C335 and its "zero point" is defined with R370/372 to 2.5V, the positive part of the rectangular wave directs T324, T326 and T334 leading, at which time power from the 15V voltage is directed to the coil. When the rectangular wave drops to zero, T325, T327 and T335 are directed leading, at which time power from the -13V is directed to the coil. The line sweep's start point is thereby shifting vertically and the scan moiré effect is diminished.



The moiré adjustment is mode specific, since the moiré in the picture varies according the resolution and picture height. A moiré adjustment value can therefore be set for every memory location, in order to optimize the moiré effect in each mode. With a new mode (unsaved mode) the moiré adjustment is set by default to zero, at which time the focus is always the best possible.

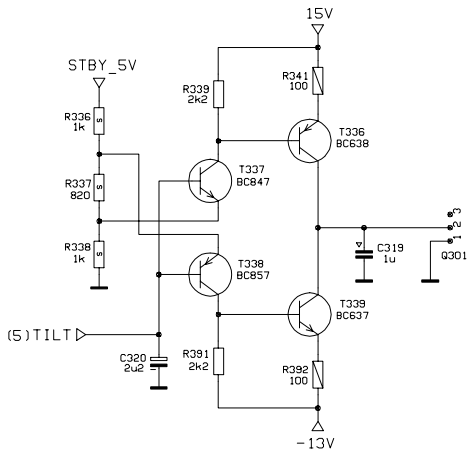
10.7 Demagnetization circuit

Magnetism remains occasionally on the metal parts of the picture tube and the monitor, which can be removed by generating a strong attenuating magnetic field with AC-current. A demagnetization coil has been installed around the picture tube for this purpose. The processor initializes the demagnetization process every time the monitor is started. The user can also initialize it through the menu by choosing the degauss-function.

When the demagnetization process begins, processor pin 12 goes up (to 5V) for approx. 125 ms. At that point, C139 charges rapidly to an approx. 5V voltage and T111 goes leading. T111 switches relay RE1 pulling and mains current starts to flow through the demagnetization coil. The PTC resistor (PTC2) connected serial with the demagnetization coil warms rapidly, the resistor resistance increases and the demagnetization current decreases, at which point the possible magnetism in the metal parts of the monitor is removed. C139 and R140 extend the relay pulling time for approx. 4.5 s and when C136 voltage has discharged through R143 to a level where T111 goes non-leading, the relay disconnects the demagnetization coil from the mains current, at which point also PTC2 is disconnected and starts cooling, in order for a new demagnetization to be initiated after a brief moment. D121's purpose is to disconnect the processor pin from T111 grid when the pin has gone down, but when C136 has not been discharged yet.

10.8 Tilt

The picture is set horizontally with the tilt-adjustment. A large coil has been wound around the picture tube neck. The DC-current fed to the coil forms a magnetic field around the coil, which causes the picture to twist. The current direction and strength is controlled by IC501/45. The amplifier stage feeding the coil is similar to the convergence and moiré stages. The adjustment value can vary between 0V and 5V, so that the middle position is a 2.5V voltage. When the adjustment value is over 2.5V, T336 and T337 are leading, and when under 2.5V, T338 and T339 are leading. Since the tilt-coil is located near the actual deflection coils, their magnetic field causes easily failures to the tilt-coil. As a result, the tilt-amplifier and coil could start to oscillate. C319 prevents this oscillation.



11. DDC

11.1 General features

Display Data Channel or DDC is a two-way data transfer channel between the monitor and the computer. It can be used for instance to transfer monitor properties data, for example the highest refreshment frequency, in order for the computer to automatically take advantage of the monitor's performance level. The DDC uses the data and clock lines (SDA and SCL) in the data transfer process.

11.2 DDC levels

When the monitor is started up and the processor gets the +5V supply voltage, it starts to feed a DDC1-level signal on the SDA line, clocked by field sync pulse VS. After the feed start, the field sync pulse frequency can be increased to 25 kHz. In this mode, clock line SCL is up. DDC1 is thus one-way data transfer from the monitor to the computer. DDC2B is two-way transfer, based on the I^2C protocol. Controlled by the computer, the monitor processor can switch to the highest level of DDC, known as DDC2AB.

11.3 Operational DDC switching

The monitor is capable of communicating in DDC1, DDC2B, and DDC2AB levels. The DDC-bus is connected to the monitor switch Q502 through the signal cable and base board, and connected to processor (IC501) pins 51 (SCL1) and 52 (SDA1). When the video card communicates on DDC1 and DDC2B levels, the transfer is controlled by IC50 on the video board. IC50 contains an EDIT-file, where the monitor maximum frequencies and resolutions are stored. When shifting to level DDC2AB (access bus), the transfer is controlled by the processor, with a different command base.

R561 and 558 are the pull-up components of the DDC-bus. R580 and R581 operate as protection components for external ESD- or other disturbances.

12. The processor

The used processor circuit (IC501) is a 8-bit SGS-Thomson monitor-use ST72T72. In addition to the normal processor functions, it contains also a block for shaping sync pulses, a DDC-block, and a I^2C bus driver for the DDC-functions. It contains also sixteen 10-bit and two 12-bit DAC (Digital Analog Converter) circuits to control DC-adjustable circuits, and eight 8-bit ADC-circuits (Analog Digital Converter) to sense DC-levels. It has also open collector circuits to control for instance the S-correction FETs. The circuit contains an internal EEPROM memory circuit, but due to lack of capacity, an extra EEPROM has been added (IC504). The external memory contains the various menu-languages, and the internal memory the various adjustment values (picture geometry etc.). In addition to these functions, the circuit has a video black level clamp pulse generator and a east/west generator (EWPCC), but which are not included in this particular monitor model.

The processor controls the monitor functions according to line and field frequency, and user settings.

12.1 Sync pulse shaping

The vertical sync pulses are connected as is to the processor (IC501) pin 27 through resistor R531. The line sync pulses are connected through the Schmitt-trigger IC502 to processor (IC501) pin 29. The higher decision level of the Schmitt-circuit eliminates the jitter access to the processor and further to the picture. R530, 532 are pull-up resistors necessary to the sync lines. D507 and D508 prevent the PC connection to the STBY_5V line through sync pulses, which could cause a processor failure in a situation where the monitor is not running, but the signal cable is connected to a running PC. The processor accepts both sync pulse polarities, and composite synchronization, at which time it separates the vertical and horizontal sync pulses in the circuit. Positive standardized vertical sync pulses are obtained from processor's pin 26, and horizontal sync pulses from pin 30. If the frequency limits are exceeded (for example horizontal sync pulses over a 125 kHz frequency), or there are no incoming pulses, the processor generates the sync pulses, which occurs for instance in a self-test situation.

12.2 Menu selection wheel

The menu selection wheel controls the adjustments and functions accomplished through the processor. When rotated, the menu selection wheel generates two rectangular sync lines, which are in a 90° phase shift.

Monostabile circuit IC506 is connected so that one of its flip-flop triggers with a rising edge, and the other with a falling edge. Up and down signals are brought from the circuit, with only one of them active according the rotation direction. The data is fed to processor's (IC501) pins 15 and 16. The processor deducts from the received data how to control the menu, either up/down or the adjustment bar cursor right/left. The wheel contains also a select switch which tells the processor (pin 20 SELECT) the user's select moment in the menu or the adjustment bar. Pressing the switch will also start the menu.

The menu is terminated by selecting EXIT from the menu, or after an inactivity period.

12.3 Other processor circuits

A crystal (10 MHz), situated between pins 33 (OSCin) and 32 (OSCout), and C517,518 and R533 are the components needed by the processor (IC501) oscillator.

Processor DACs (DAC 0 - 17) are pulse width modulation typed (PWM). Their output voltages are pulse shaped, and the pulse width defines the DAC DC-voltage after the RC-filtering. A wide positive pulse equals a higher voltage. The serial resistor and the capacitor are used for the filtering, for instance the width DAC (Width, DAC7, pin 10) filtering components are R514 and C509. Since the adjustment in question is sensible to a possible ripple (voltage altering), another filtering circuit is used: R559, C528. DAC0 and DAC2 are open collector typed, so they necessitate pull-up resistors R556 and 577.

DA1 generates the contrast voltage maximum value going to the video board, and the corresponding filtering components are R505 and C519.

S-capacitor controls PA 0-6, pins 37-43) are open collector typed, so their pull-up resistors are R536-541 and R582. R542-547 and R583 are used to generate delay to the S-correction FETs disconnection (the connection is delayed). Without these resistors, the S-capacitor disconnects more rapidly (since it is accomplished through high-impedance pull-up resistors). In a mode change situation, this might result to a situation where all the capacitors would be disconnected for a brief moment, thereby increasing the dynamic focus to a very high level, which is not desirable.

By using serial resistors, the FETs disconnection is made slower (connection time is not as much influenced), resulting to a situation where at least one FET is always leading, limiting the dynamic focus voltage increase.

The self-test and input select signals generate data to the processor about which video input is selected, and if the cable is connected to the monitor (only D-connector input). The processor performs the needed deductions according the processor pin 14 (PB6, analog input) voltage.

Voltage in pin 14	Status
over 4.0V	BNC selected (D-connector cable off)
2.7V…4.0V	BNC selected (D-connector cable on)
0.8V…2.7V	D-connector selected, cable off
under 0.8V	D-connector selected, cable on

For instance, when the user has selected the BNC-input (switch SW602 open) and the D-cable is connected to the monitor, voltage division IC501/14 is formed through resistors R510, R519 and R518.

If the monitor is started so that IC501 does not get the necessary sync signals, the processor changes to the so called Self-test mode. At that point, the processor starts to run on constant frequency, generates horizontal and vertical pulses (approx. 80 kHz and 75 Hz) showing a self-test screen. The user can determine that the monitor is functioning, but only a cable has been disconnected or the video input has not been properly selected.

13. Video amplifier SMY039/SMH144

The video amplifier is composed of two modules, of which the SMH-module contains the picture tube base connector, filter- and protection components. The SMY-module is the actual video amplifier.

The video amplifier is composed of two input connections and their select circuit, the on-screen menu (OSM) summing circuit, the OSM circuit, three separate pre-amplifiers, three buffer amplifiers, an output amplifier hybrid, three black level/brightness adjustment and clamping circuits, a digital /analog converter circuit (DAC), and the DDC-circuit.

The video amplifier has been designed to control a 21" picture tube up to a point/dot frequency of 270 MHz. The video amplifier adjustments are accomplished through the I^2C bus.

The video amplifier (SMY039) is composed of three separate amplifiers (red, green and blue). The reference channel in this manual is the red channel.

13.1 SMY039

13.1.1 Input connection selection

The monitor has two signal inputs (BNC and Dsub), which are terminated to 75Ω for the video signals (R101 and R102). The input selection is accomplished with IC10 (BA7657F). The circuit connects the selected video (IC10/1 and 7), vertical- (IC10/12 and 13) and horizontal sync pulses (IC10/24 and 23). The circuit input side is AC-connected, with additionally ESD-protection zener diodes and diodes. The selection is done by the user with a switch on the front panel, whose position data is fed to IC10/16.

The selection circuit contains additionally a G-channel sync pulse (sync on green) separation. The separation stage input is in pin 18, which is connected through C14 to the G-channel output. The H/V sync pulses (comp sync) are brought from pin 17. If separate horizontal sync pulses are coming simultaneously from the driver, the pulse separator will not produce the H/V sync pulses from the circuit.

13.1.2 OSM summing

The OSM messages are summed to the actual video signal multiplexer with EL4331 (IC70). The AC-connected signal black level is clamped to -0.7V voltage with D108, D109, and R116, R144. For the duration of the OSM messages, the circuit's A-input pin (IC70/12) is selected with a TTL-level selection signal brought to pin 16. Video coming from the PC or any other driver is connected to the selection circuit's B-pin (IC70/11). The selection signal is generated in the OSM-circuit (IC60) and summed to IC70 selection pin 16 with diode D60. When the monitor is in an unrecognizable mode (for instance between mode changes), the OSM-input is selected from IC70, at which point the actual video signal display is blocked, and non-synchronized pictures are not visible. This selection signal is brought from the processor and summed to IC70 selection pin 16 with diode D61. When the selection signal is "1", the multiplexer OSM-input pins are selected.

13.1.3 OSM circuit

The monitor's adjustments are accomplished with the OSM-window, generated by the LSC4386 OSM-circuit. OSM circuit IC60 is controlled by the processor through the I^2C bus.

The sync signals are brought from the deflection stage, at which point they are independent from the sync signals coming from the driver (PC). The vertical sync pulses are brought to OSM circuit pin 10 and the horizontal sync signal to pin 5.

The circuit contains a voltage controlled oscillator, with external components at pins 1-4. The OSM-video timed TTL-level blanking signal is brought from circuit pin 12, and fed to multiplexer (IC70) pin 16.

The TTL-level OSM signal is brought from IC60 pin 15, and fed through voltage divider R141, R142 and R143 to multiplexer input pin 12. The OSM video output is twin level, at which point two brightness levels are generated for the OSM-window. When the output is TTL-level, the previous voltage divider sets the video level to approx. 600mV, at which point the OSM cursor brightness is slightly less than the actual video brightness (high intensity). When the output is high impedance level, the voltage divider is used to set the video approx. 450mV, at which point the OSM-window is slightly less bright than the cursor brightness (low intensity). The selection is done by software through the I^2C bus.

13.1.4 Pre-amplifier

The used pre-amplifier is a one-channel National LM2202 circuit, with a band width of 230MHz. The pre-amplifier circuit contains an input amplifier, a contrast adjustment stage, a keyed black level clamp circuit, an adjustable amplifier stage and an output circuit. The circuit operates on a 12V supply voltage.

The video signal from the multiplexer is brought through switching capacitor C101 to the circuit input pin 6. The input pin is pre-amplified internally to a 2.6V voltage.

All of the pre-amplifier pins 1 are connected together, as are the pins 2. At that time, IC100 functions as the contrast adjustment master circuit, thereby achieving the best possible result in the contrast tracking (the picture color temperature is constant, regardless of the contrast adjustment position).

The contrast adjustment voltage is controlled with an adjustment potentiometer located on the monitor's front panel. The adjustment voltage is brought to IC100 pin 8 and is 2V at its maximum, at which point the amplitude in the output (pin 17) is approx. 5Vpp.

To achieve the wanted color temperature, the amplification must be adjusted specifically for each channel. The pre-amplifier is DC-adjustable, and the adjustment voltage is brought to pin 9. The adjustment voltage is brought from the DAC TDA8847 (IC30/16). The adjustment functions are both factory/maintenance adjustments, as well as a user adjustments.

A negative polarity black level clamp keying pulse is brought to circuit pin 14 during the back porch clamping. The keying pulse length is approx. 460ns.

During the keying, the circuit compares the output DC-level to the pre-set reference voltage, and corrects the output DC-level with internal comparators. The reference voltage, generated with resistors R105 and R106, is fed to all the pre-amplifiers' pins 19.

An output signal is brought from the circuit output pin 17, with an amplitude of approx. 5.0V, when contrast is at its maximum, and when the beam current limiter does not limit the amplitude (for instance the window picture). The output DC-level is approx. 1.0V.

R111 is the output circuits output resistor, after which the output signal is fed to the buffer stage input through resistors R150 and R151.

13.1.5 Buffer stage

The pre-amplifier circuit cannot directly control the current controlled output hybrid, requiring use of a separate buffer amplifier between the pre- and output amplifiers. The buffer amplifier is a DC-connected, complementary type amplifier composed of two emitter followers. T150 (BFQ131;NPN) emitter follower buffers the positive current peaks. Correspondingly, T151 (BFQ151;PNP) emitter follower buffers the negative current peaks. Diodes D150-D152 decrease the DC-level in one pre-amplifier DC-level adjustment, so that the black level output amplifier output is approximately 70V.

Zener diodes DZ81 and DZ89 decrease the buffer stage's negative supply voltage, so that the transistors maximum voltage stays within the approved limits.

13.1.6 Output stage

The output stage output resistor is R120, parallelly with RC-chains R118, C118 and R122, C120 forming the signal path for high frequency components.

These components are used to adjust the alteration speeds and stabilization periods after the alterations to the wanted level.

The used output stage is a Philips CR6927 (IC2) feedback current controlled three-channel hybrid, with a voltage amplification of approximately 12 (adjusted with input resistor R120). The hybrid band width is 120MHz with a 40V amplitude. The DC-connected output stage operates at a 80V supply voltage, and the output (pin 4) black level is set to 70V as previously mentioned.

The RC-chain (R119,R121 and C122) between the hybrid output and input pin, functions as a smearing correction, preventing the generating of post-control "tails".

13.1.7 Black level clamp- and adjustment circuit

After switching capacitor C122, the video signal black level must be clamped channel by channel, in order to render the background frame's color balance to the right level. In the black level clamping, a keyed diode clamping is used during the back porch (back porch clamping).

The cathodes' black level adjustments are accomplished through the I^2C bus, at which time the black level adjustment voltage is brought to the DAC-circuit (IC30) from pin 13. The adjustment voltage is

brought to transistor T102's base -which operates as a current generator- through resistor division R36, R41, R42 and D40. By adjusting transistor T102's collector current, buffer transistor T101 emitter voltage is altered; the cathode's DC-level is clamped at this point.

The keying pulse polarity is reversed with transistor T90 and amplified with FET TF90 to 140V. During the keying pulse, diodes D105 and D106 are leading, at which point the cathode DC-level is adjusted to T101 emitter voltage. The black level voltage is adjustable at a range of 103-130V (the brightness adjustment affects the previous voltage).

13.1.8 Brightness adjustment circuit

The brightness adjustment is used to adjust the cathodes' black level voltages through black level adjustment circuits, emphasized with typical channel amplitudes, at which time the color temperature is preserved as the correct brightness function. The emphasis is accomplished with resistors R133, R134, R233, R234, R333 and R334.

The user-controlled brightness adjustment voltage is brought from the potentiometer in the monitor front panel. Bus-controlled DAC IC30/9 can be used additionally in factory- and maintenance adjustments.

The auxiliary adjustment voltage is summed to the brightness adjustment line with diode D50.

The brightness adjustment voltage is summed to the black level adjustment voltage with current generator T103. The adjustment voltage amount on the cathode is approx. 11V.

13.1.9 DAC circuit

The amplification- and black level adjustments are accomplished through the I^2C-bus by converting the processor adjustment data to analog form with converter circuit TDA8447 (IC30). The circuit is an 8-channel, 8-bit, 5V supply voltage digital/analog converting circuit.

The black level adjustments and brightness auxiliary adjustment are solely factory/maintenance adjustments. The user color temperature adjustment affects the black level adjustment voltage, so that the frame color temperature is adjusted to the selected value. The amplification adjustments function as factory/maintenance adjustments, and user adjustments through the OSM.

13.1.10 White spot suppression

When shutting down the monitor, the white spot generating is prevented by pulling rapidly the G1-grid to a negative voltage with the blanking amplifier located on the base board. Diode D80 prevents the 190V discharge from capacitor C80, at which time, after the blanking, the cathode DC-level increases from the black level value through pull-up resistor R125.