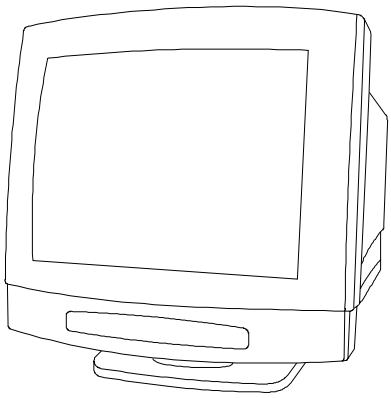
Circuit Description

	Chassis 447Z

17” High Resolution Color Monitor



Circuit Description
Circuit Diagrams

When re-ordering manuals, please quote the model name and part number	**ZB1567** 02.97

2. Introduction

2.1 General features

This is an autosync-type microprocessor controlled 17 " color monitor. The horizontal frequency range is 31…72 kHz and the vertical frequency range 48…120 Hz, with a maximum resolution of 1280 x 1024. The monitor has been designed to operate with separate TTL-level horizontal and vertical sync pulses, and with composite sync.

The monitor operates on a mains voltage range of 90…264 VAC 50/60 Hz. The power supply of the monitor has been designed to operate on the whole voltage range, so there is no need for a separate voltage switch.

The monitor has VESA-standard Power Save modes.

With the help of a membrane keypad located on the front panel of the monitor, the user can adjust various factors affecting the image quality, like the image size, geometry, color temperature etc.

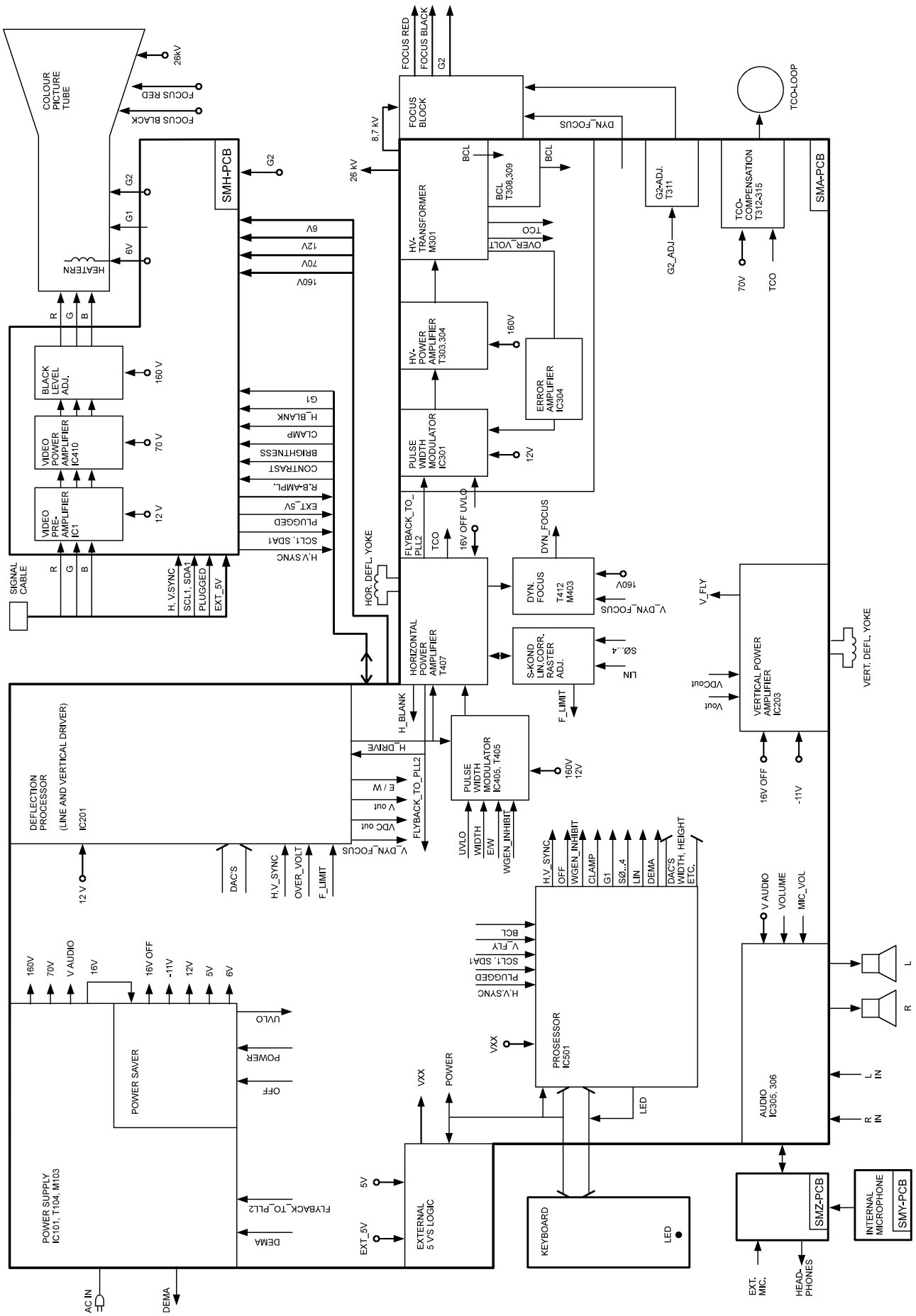
The monitor recognizes the used mode with the help of the V- and H sync pulse frequency and the polarity of the V-sync pulses. If a memory location has been created for the setting, that is, if it is a so-called factory setting, the picture size and geometry are automatically adjusted to the optimum. If the monitor does not recognize the used setting, that is, if the setting has not been optimized, the user can easily adjust himself the picture with the membrane keypad. This "new" setting is automatically saved in the monitor's memory to be ready for the next session.

The monitor does not have a switch cutting off the mains voltage, but a so-called sleep switch which does not cut off the monitor's power supply, but only some of the voltages in the secondary side of the power supply.

Important! The monitor's power supply is operational when there is a mains current available. For instance, the 160 V voltage is always on, even if the monitor has been switched off with the sleep switch. It is thus important to cut off the mains current by removing the plug from the socket when doing repair jobs**.**

2.2 The block diagram

The monitor's power supply and deflection parts block diagram is represented in picture 1. It contains the following operational blocks:


COLOUR PICTURE TUBE
26kV
FOCUS RED
FOCUS BLACK
HEATERN
G2
G1
6V
SMH-PCB
SIGNAL CABLE
R
G
B
H. V.SYNC
SCL1, SDA1
PLUGGED
EXT_5V
BLACK LEVEL ADJ.
VIDEO POWER AMPLIFIER IC410
VIDEO PRE-AMPLIFIER IC1
160 V
70 V
12 V
6V
12V
70V
160V
G1
H_BLANK
CLAMP
BRIGHTNESS
CONTRAST
R.B-AMPL.
EXT_5V
PLUGGED
SCL1, SDA1
H.V.SYNC
HOR. DEFL. YOKE
FOCUS RED
FOCUS BLACK
G2
FOCUS BLOCK
8.7 kV
26 kV
DYN_FOCUS
TCO-LOOP
HV-TRANSFORMER M301
BCL
BCL T308,309
OVER_VOLT
TCO
G2-ADJ. T311
G2_ADJ
TCO-COMPENSATION T312-315
70V
TCO
SMA-PCB
HV-POWER AMPLIFIER T303,304
160V
ERROR AMPLIFIER IC304
PULSE WIDTH MODULATOR IC301
12V
FLYBACK_TO_PLL2
TCO
16V OFF
UVLO
DYN. FOCUS T412 M403
160V
V_DYN_FOCUS
HORIZONTAL POWER AMPLIFIER T407
S-KOND LIN.CORR. RASTER ADJ.
SØ..4
LIN
F_LIMIT
H_BLANK
H_DRIVE
PULSE WIDTH MODULATOR IC405, T405
160V
12V
V_FLY
VOut
VDCout
VERTICAL POWER AMPLIFIER IC203
VERT. DEFL. YOKE
16V OFF
-11V
DEFLECTION PROCESSOR (LINE AND VERTICAL DRIVER) IC201
12 V
DAC'S
H.V_SYNC
OVER_VOLT
F_LIMIT
V_DYN_FOCUS
VDC out
V out
E / W
FLYBACK_TO_PLL2
UVLO
WIDTH
E/W
WGEN_INHIBIT
H.V_SYNC
OFF
WGEN_INHIBIT
CLAMP
G1
SØ..4
LIN
DEMA
DAC'S WIDTH, HEIGHT ETC.
BCL
V_FLY
SCL1, SDA1
PLUGGED
H.V.SYNC
VXX
PROSESSOR IC501
LED
V AUDIO
VOLUME
MIC_VOL
AUDIO IC305, 306
L
R
L IN
R IN
160V
70V
V AUDIO
16V
16V OFF
-11V
12V
5V
6V
POWER SAVER
UVLO
POWER
OFF
POWER SUPPLY IC101, T104, M103
FLYBACK_TO_PLL2
DEMA
AC IN
DEMA
VXX
POWER
5V
EXT_5V
EXTERNAL 5 V'S LOGIC
KEYBOARD
LED
SMZ-PCB
INTERNAL MICROPHONE
SMY-PCB
EXT. MIC.
HEAD-PHONES

Picture 1

2.2.1 The power supply

Produces the voltages needed by the monitor. Contains also the VESA Power Save and picture tube demagnetizing functions. The operational frequency has been synchronized to the horizontal deflection frequency.

2.2.2 The power save function

This function lowers the monitor's power consumption in VESA Power Save modes. The function is composed of electronics and software.

2.2.3 The deflection driver

Forms a correctly timed control signal (compared to the incoming sync pulse) for the horizontal output stage. Controls the vertical output stage and forms the vertical frequency picture geometry correcting voltages and the vertical frequency control voltage for the dynamic focus. Blanks the screen during mode change situations. Controls the high voltage.

2.2.4 The width control circuit

Forms the proper supply voltage for the horizontal output stage. Sums to this voltage the required geometry correcting voltages (E/W and trapezium).

2.2.5 The high voltage generator

Forms the regulated 25 kV high voltage as well as the focus- and G2-voltage. Synchronizes the power supply.

2.2.6 The vertical output stage

Forms a proper current for the vertical deflection coil. Forms the vertical blanking pulse.

2.2.7 The horizontal output stage

Forms the current needed by the horizontal deflection coil, the DC-current needed by the frame centering and the linearity and S-correction. The line fly-back pulse (FBP) formed by the stage is used to the controlling of the high-voltage generator and the deflection coil and to the forming of the line blanking pulse.

2.2.8 The blanking circuit

Forms the vertical and horizontal blanking pulses, blanks and narrows the screen during a mode change situation.

2.2.9 Other functions

Auxiliary functions are, for example:

1. A beam current limiter circuit, which limits the maximum beam current to the desired level.
2. A TCO-compensating circuit, which forms a TCO compensating pulse used to reduce the electric field emitted by the monitor.
3. A reset-circuit, which forms the reset pulse needed by the processor. Forms a pulse also in a picture tube cross-over situation, which decreases the risk for the processor to fail.
4. A clamp pulse forming circuit, which forms the black level clamp pulse needed by the video.
5. A Moire-adjustment circuit used to minimize the Moire on the picture.
6. A demagnetization circuit used to demagnetize the metal parts of the monitor.

2.2.10 DDC

Display Data Channel or DDC is a two-way data transfer channel between the monitor and the computer. It can be used, for example, to transfer information about the monitor features, the maximum refreshing frequency, so that the computer can optimize the monitor features automatically.

2.2.11 Audio stage

The monitor has optional audio part, which contains a stereo audio amplifier, speakers, an internal microphone and a microphone amplifier. Additionally, there is a headphone plug and an external microphone plug.

2.2.12 The microprocessor

Controls the monitor functions according to the horizontal and vertical sync pulses and the orders given by the user.

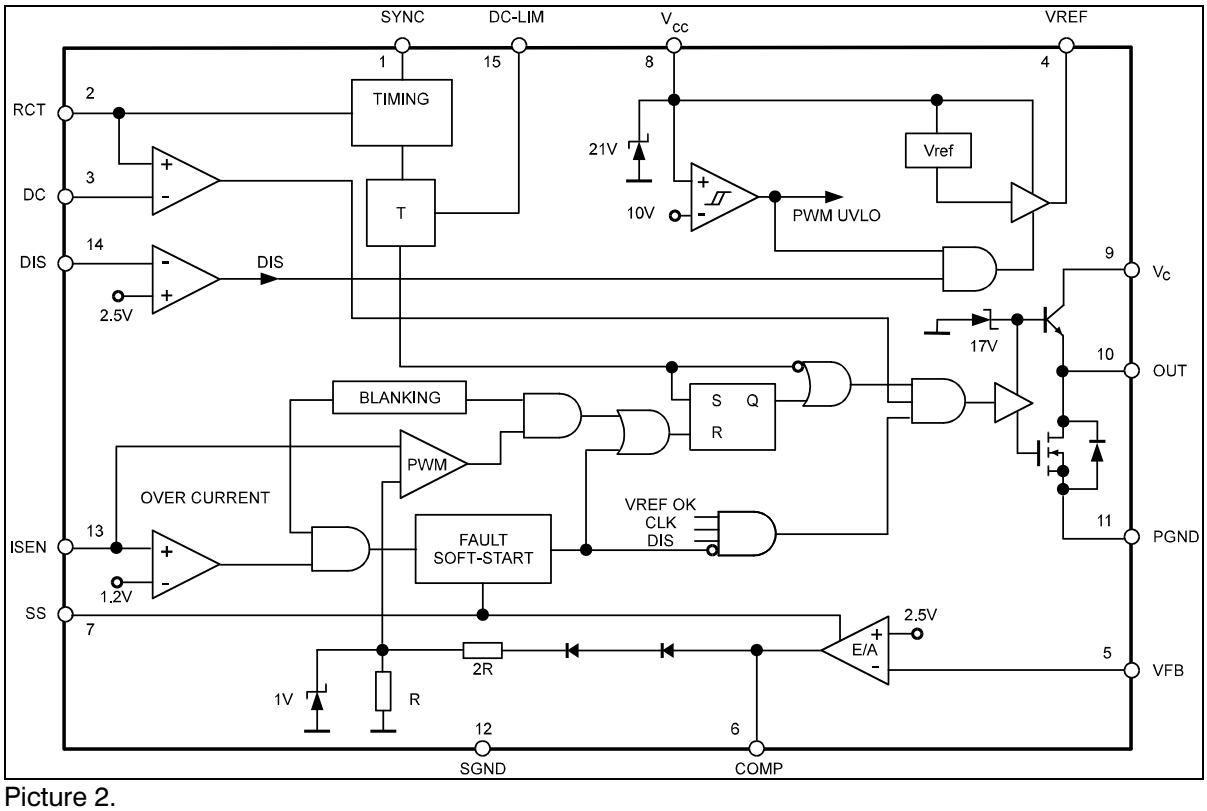
2.2.13 The video amplifier

Amplifies the approx. 0.7 V RGB signals coming from the video card through the signal cable to approx. 35 V drive voltages appropriate to the picture tube.

3 The power supply

3.1 General features

The voltage supply is a secondary regulated, current mode, continuous/non-continuous Fly-back type switch mode power supply, with an operational voltage range of 90…264 VAC.
The regulation from the secondary has been achieved with an opto-isolator. The operational frequency (switch mode frequency) is 25…72 kHz and it is synchronized to line frequency. The power supply operates in a non-continuous operational mode using low primary currents and converts to continuous mode when the load increases.
The voltage supply is based on a SGS-Thomson IC-circuit L4990 (current mode PWM). The block diagram is shown in picture 2.



Picture 2.

The power supply's control circuit L4990 is based on the popular UC3842 circuit and contains a differential amplifier, a RC-oscillator, a current measuring comparator, a 5V reference voltage, an output stage for the control of the FET, and an under voltage lockout. In addition to the above mentioned functions of the UC3842, the circuit has also a programmable Soft start function, a two stage over current

protection, a lockout circuit of the pulse ratio (not used in this monitor, since the pulse ratio has been adjusted to 100%) and an over voltage disable function. With these functions, the power supply's operation is more reliable in various error situations.

3.2 The start-up

The supply voltage is rectified with diodes D101…D104 and filtered with capacitor C110. IC101 gets the current needed for start-up through T103, T104, R114, R120 and R107. When C121 voltage rises to 16V, IC101's under voltage function allows the IC start-up. At that time, the IC oscillator starts-up and FET T107 goes leading. Simultaneously, the capacitor of pin 7 of the IC (soft start) starts to charge with standard current of 20 μA. The current through mains transformer M104 primary coil (pins 2 and 18) and the FET starts to grow until the voltage loss over current measurement resistors R133, R134 rises to the same level as the soft start capacitors (C131) voltage in pin 7, which is clamping the output voltage of the internal current measurement comparator (E/A on the block diagram). At that time, the current measurement comparator directs the FET to off-mode and the energy charged in the primary coil is transferred to the secondary coils and from there on through the secondary diodes to the secondary capacitors. After this, the IC101 oscillator again drives the FET T107 to conduct and so on. The soft start capacitors voltage rises all the time, growing also the pulse ratio, so that in every period the current through the primary coil is higher. The pulse ratio is thus very low at the beginning of the start-up, therefore rising slowly the voltages at the secondary. When the soft start capacitor has been charging to its maximum, the soft start circuit does not limit the function of the power supply. The IC101 oscillator directs the T107 FET to leading and so on. This goes on as long as the secondary capacitors have been charged to the right voltage. At that time, the feedback starts to control the IC101 differential amplifier, which controls the primary current through the FET (look 3.4 current regulation).

When IC101 is operational, its pin 4 has a 5V voltage. This voltage drives the transistor T105 leading through R121. At that time, the voltage in transistor T104 base decreases under the supply voltage of IC101, so that transistor T104 goes non-conducting. Simultaneously, the current through resistors R114 and R120 is removed and IC101 gets its supply voltage solely through the primary's auxiliary coil (pins 8 and 20) and diode D106. If the IC's supply voltage drops under 10V, IC101's internal under voltage lockout circuit switches off the IC and thus also the power supply, so that the start-up sequence starts from the beginning.

3.3 The synchronizing

The power supply is synchronized to horizontal deflection frequency. The positive line fly-back pulse (FLYBACK_TO_PLL2) coming from the horizontal deflection output stage is directed with R199 and D145 through the opto-isolator (IC107) to the synchronizing pin 1 of IC101. C172 is used to accelerate the synchronizing (smaller delay) and the pulse is optimized for the opto-isolator with R190 and R127. The rising pulse edge going over R127 is triggering the IC oscillator thus directing FET T107 to leading. The free oscillation frequency of the power supply's oscillator is controlled with components C126 and R126, which control the power supply's free oscillation frequency when the deflection stage is not running (for instance a power-off situation). This free oscillation frequency is approx. 25 kHz.

3.4 The voltage regulation

The voltage feed-back information is taken from the 160V voltage, which is dropped to the reference voltage level 2,5V of regulator T109 with resistors R153 and R152. Regulator T109 is composed of an inverting amplifier and a reference voltage.

Function description through an example:
If the 160V voltage is increasing (the charge load decreases), the T109 grid voltage increases. Then the current through T109 and R147 increases as well. This current increases the voltage loss of resistor R147, at which time the IC102 (opto isolator) diode current decreases. This drives the current of transistor IC102 and resistor R105 to decrease, which makes the voltage of IC101 pin 5 (opto isolators negative input) to rise and the output voltage of the opto isolator to drop. The output voltage of the opto isolator functions as the reference voltage of the current measurement comparator, at which time the comparator decreases the primary current, thus decreasing as well the 160V secondary voltage.
The fast current changes are summed to the feed-back with capacitor C143 and the power supply is reacting more rapidly to the charge changes.

3.5 Slope compensating

The primary current pulse ratio cannot exceed 50%, so the IC101 switching contains slope compensating, so that the stability of the power supply would be secured in all situations. The saw-tooth wave of IC101 oscillator (from C126) is summed to the input voltage of the current measurement comparator (IC101 pin 13) with T124, R123, C127, R124 and C128.

3.6 The over current control

The circuit L4990 contains an over current control circuit, which prevents the secondary voltages to rise too high in a failure situation, thus preventing the electrolyte capacitors from being damaged. In this particular situation, they would cause an abundant quantity of smoke, which is not acceptable, even in a failure situation.
In a normal situation, when the 160V voltage is at the right level, the IC101 supply voltage is approx. 16V (pin 8). At that time, the IC101 pin 14 (DIS) voltage is approx. 2.1V with the help of resistors R170 and R171. If the device fails in such a way that the regulation does not work and secondary voltages rise too high (over 190V), the IC101 pin 14 voltage increases as well. When its voltage increases to 2.5V, pin 10 of the IC (FET control) goes down immediately and the IC oscillator shuts down. At that point, the power supply of the monitor is completely shut down and the secondary voltages decrease and will not rise too high even for a moment.
In this situation, the circuit's reference voltage (5V on pin 4) goes down, so that T105 is saturated and its collector voltage goes up. After this, T103 and 104 go leading and feed current to IC101. Its voltage on pin 8 increases to approx. 25V because a zener-diode inside the circuit limits the voltages to that particular factor. The IC will not restart in an over current situation until its supply voltage has decreased under 10V and on the other hand, T103 and 104 continue to feed current to the circuit (voltage is maintained at 25V) the situation is latched, the power supply will not start without a separate action. This situation is easily noticeable, since the LED is not lit (no voltages in the secondary) and the IC101 supply voltage is approx. 25V.
This situation can be discontinued only by switching off the supply power for about 2 minutes (at which time the C10 and C121 voltages is discharged). The membrane key on the front panel of the monitor is not operating but the only way is to unplug the mains cord. This is not a problem in practice, since this over current situation is a sign of a serious failure, so the monitor has to be repaired anyway.
C125 operates as a filtering capacitor, thus preventing effects of external disturbances to the circuit.

3.7 The primary current lockout

The circuit has a two stage primary current measurement and protection function. When the power supply is functioning normally (the maximum pulse voltage of R133 and 134 is approx. 1V), the feed-back information coming from the secondary directs the pulse ratio of the primary switch with the current measurement comparator, and thus also the secondary voltages. The voltage regulation operates as mentioned before.
If an over current situation occurs and the primary current has time to rise to a level where the current measurement resistors (R133 and 134) voltage is over 1.2V, the circuits over current protection function starts up. At that time, the circuit cuts off immediately the control of the primary switch (the circuits pin 10 goes down at once), and discharges the soft start capacitor at pin 7 (C131). At that time, the circuit starts the next period with a very short control pulse, and if the over current situation is still on (R133 and 134 voltage still over 1.2V, that is, plenty of primary current), the C131 voltage must rise to 5V before it is discharged, and the primary switch is kept non-leading all this time (the power supply is shutdown and there is no primary current). In an over current situation like this (for example a component of the secondary side in short-circuit), the circuit gives current to the secondary for a very brief moment and is shut down most of the time, so there is not much power going to the secondary. This way, the over current components' temperature does not rise too high and additional damages and smoke are avoided. If the over current situation is only temporary (for example an error in a mode change situation), the monitor is operating normally without that the user even notices any abnormality.

3.8 The secondary current lockout

The 160V and 70V secondary coils are serial connected, so that the current of both voltages goes through R159 and 160. In an over current situation, the voltage loss of these resistors increases higher than 0.7V, at which time T110 goes leading and gives extra current to the feed-back information with R154. At that time, the voltage of regulator T111 grid increases and with feed back information the power supply's output voltages decrease as well. Following this, also the voltage of the primary's auxiliary coil (pins 8 and 20) decrease, at which time the supply power of IC101 decreases under 10V. At that time, the under current lockout of the IC prevents the IC and the power supply from operating. The power supply tends to restart itself after a moment and if the over current situation is still there, the lockout function of the secondary current is repeated.
The smaller secondary voltages are protected from over current with inflammable resistors or fuses, which burn and cut in an over-current situation.

3.9 The UVLO signal

The UVLO signal (transistor T120) is used to stabilize the functioning of the field deflection and the high-voltage generator in start and shutdown situations of the monitor. The UVLO signal is activated when the Power switch is pressed or if the 16VOFF voltage drops under 13V, for instance when in a supply power failure or when the device goes to Power Off-mode.

When the 16VOFF voltage is under 13V, the voltage in T121 base is under 0.7V, so it is not leading. The T121 collector and T120 base is therefore up, so T120 is leading and decreasing the UVLO signal. When the 16VOFF voltage rises and exceeds 13V, T121 goes leading and T120 non-leading, so the UVLO signal goes up.

When the UVLO signal goes down due to, for example, a power failure, it resets the width modulator IC401 through diode D416 by pulling IC401 pin 13 down. At that time, the power feed to the line deflection driver is cut off. Simultaneously, capacitor C405 is discharged and the image width adjusts to minimum. Deflection driver IC201 gets still supply power (12V is dropping but is still high enough for the functioning of the driver), and gives H-drive signal to the line deflection output stages transistor T407. This goes on until the 12V voltage has dropped under 7.5V at which time IC201 shuts down. During this time, the transistor T407 of the line deflection output stage discharges the S-capacitors. This way it is being made sure that in the next start up, the line deflection stage does not start up with a too high supply power (S-capacitor voltage).
When the UVLO signal goes down, the T306 base goes to approx. 0.7V with D316. Following this, the T304 grid cannot rise over 1.4V, so it does not go leading, and the high voltage generator shuts down. This way, the proper functioning of the high voltage generator during power failures is secured.
The UVLO signal is also summed to the blank signal (V_BLANK) with diode D205, thus preventing the appearing of a fuzzy image (not synchronized and so on) in start and shutdown situations.
Additionally, the UVLO signal is switched with D141 to the DEMA (demagnetizing) function. When processor IC501 goes to a start up situation (when 5V is too low) it rises its start pin, and this would start the demagnetization also in shutdown situations, which is not desired. This failure situation is prevented with D141.

4 The power save function

4.1 General

The power supply contains the switches which are used by the processor to control the various power save modes of the monitor. In practice this means that the supply voltages of certain blocks of the monitor are cut off, at which time the monitor power consumption is decreasing. Additionally, the video amplifier is directed via brightness and contrast lines to a mode where power consumption is the lowest. The switching for the disabling of IC101's start up current is also part of the power save function.

The processor monitors the incoming sync pulses and directs the monitor through VESA Power Save Management Standard as follows:

4.2 On-mode

If both line and field pulses are brought to the monitor, the processor interprets it as ON-mode. This mode corresponds to normal use.

4.3 Stand by-mode

If line sync pulses are missing, the processor interprets it as Stand-by mode. At that time, the processor decreases the brightness and contrast line and the monitor image is black. Simultaneously, the processor starts up an internal sync pulse generating and the line deflection frequency is at 64 kHz. The power save is small compared to the normal mode.

4.4 Suspend-mode

If field sync pulses are missing, the processor interprets it as Suspend-mode. In Suspend-mode, the processor pulls down the WGEN_INHIBIT line (IC501 pin 37). When this signal is down, D427 pulls down IC401 pin 13 with D416, at which time the width modulator goes to static clear-mode, and does not give any control pulses to the width switch mode. Because the width switch mode is not functioning, the line output stage does not get any supply voltage and is thereby going off and cutting off the high voltage generator. The supply voltages of the field output stage are not cut off in this mode. 12 V is not cut off either, so the field oscillator and line oscillator are still running just like at ON-mode. The filament current can flow normally, so the return from this mode to ON-mode is rapid: the image comes back in approx. 1 second.

In suspend-mode the power save is quite important, the consumption being approx. 22 W.

4.5 Power off mode

If both sync pulses are missing, the processor interprets this as Power off-mode. In power off-mode, the processor pulls up the OFF line (IC501 pin 22). When this line is up, T126 is leading, and its collector pulls down the T127 grid. T117 goes non-leading and the 16VOFF-voltage from the field output stage is cut off. T108 goes also non-leading with zener diode DZ108, because its grid voltage, which normally is approx. + 4V (source is at -11V, so the source-grid voltage is approx. 15V), drops to approx. -11V. Because the FET source is also at -11V, the source-grid control voltage is 0V, at which time the -11V from the field output stage is cut off. At this time, the field output stage does not consume any power. Because 16VOFF is cut off, the 12V output voltage of regulator IC104 is also cut off. Due to this, all 12V circuits (among others IC201) are inactive, and do not consume any power. Because the filament regulator IC11's input voltage (16VOFF) is cut off, the filament voltage is also cut off.

At this point, the monitor's power consumption is typically approx. 4W.

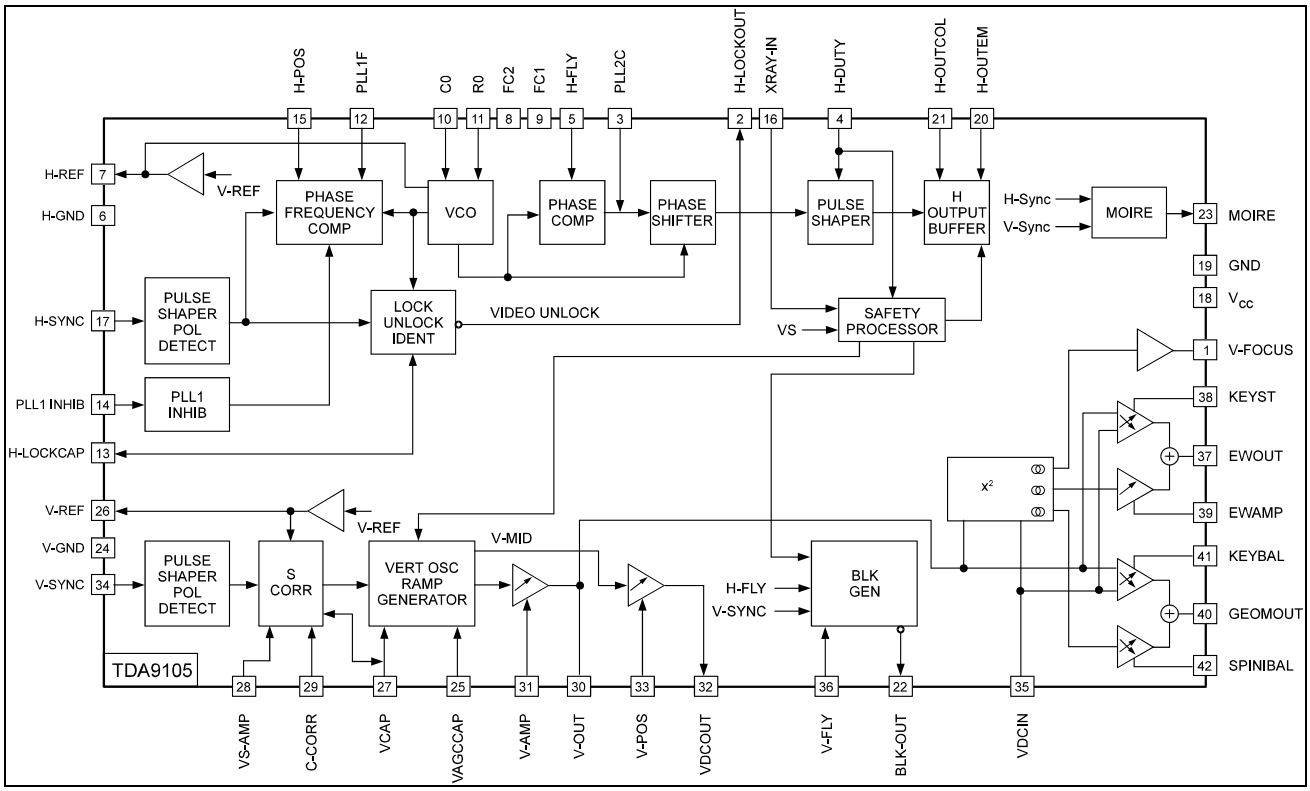
5 The deflection driver

5.1 General

The used deflection driver is a SGS-Thomson circuit TDA9105. This circuit contains stages to control both the line deflection and the field deflection. Additionally, there is basic picture geometry adjusting functions. Other functions are the x-ray lockout circuit, the under voltage lockout, the blanking output and the field frequency parabola for the control of the focus. The operational frequency range of the circuit is 15-125 kHz and the supply voltage range 10-13.2V. The circuit is packaged in a 28-pin DIP box.

5.2 Block diagram

The TDA9105 block diagram is represented in picture 3



Picture 3

Two separate fields can be observed in the block diagram: line frequency and field frequency blocks. Line frequency blocks form an “H-drive” signal to the line deflection output stage and the field frequency blocks form a control voltage to the vertical deflection output stage. Additionally, the field frequency blocks form the picture geometry adjusting voltages. The circuit has also common blocks for the line and field frequency parts, like the blanking block and the safety function block “safety processor”.

5.2.1 The line frequency blocks

The line frequency blocks form two stage locks after another: PLL1 and PLL2.

PLL1 is composed of the phase/frequency comparator and the VCO.

The comparator keeps the VCO frequency at the same level as the incoming sync pulses frequency. The saw tooth wave formed by the VCO (measured from pin 10) is phase adjustable against the incoming sync pulses (pin 17) with a DC-voltage brought from pin 15. The circuit has been adjusted in such a way that when the control voltage is at the mid position (4V), the middle of the fly-back pulse is 12.5 % from the phase time behind the trailing edge of the sync pulse. The whole adjusting range (2…6V in pin 15) is +-12.5%.

The PLL1 phase comparator function can be prevented with a positive voltage brought to pin 14. At that time, the VCO voltage is not dependent on the incoming sync pulses. This method can be used in a situation where the influence of non desired sync pulses to the deflection frequency has to be prevented, when using a composite sync pulse, for instance.

PLL1 contains also a detector, which indicates whether the phase lock is locked or not to the incoming sync pulse.
If the phase lock is locked, the voltage in pin 13 (H-lock cap) is high (exceeds 6.5V) and the internal transistor (open collector) in pin 2 is non-leading, that is, pin 2 is up. If the phase lock is not locked, the voltage in pin 13 drops under 6.5V and the transistor in pin 2 is leading, so pin 2 is down.

PLL2 compares the phase of the incoming line fly-back pulse to pin 5 and the VCO. If the phase of the line fly-back pulses is changing compared to the VCO phase, for example for the heat drifting of the deflection transistor, the output voltage of the comparator in pin 3 is changing, which in turn changes the resolving levels of the internal comparators and through that, the phase of the H_Drive signal, thereby readjusting the fly-back pulses phase to the right level. Phase lock 2 is thereby compensating the various delays emerging from the deflection output stage.

The H_Drive signal is brought out either from pin 20 or pin 21. Pin 20 is the emitter of the output transistor and pin 21 is a collector. The H-drive signal pulse ratio can be adjusted by changing the DC-voltage of pin 4. The adjusting range is 34%…56%.

5.2.2 The field frequency blocks

The circuit's vertical part contains a vertical oscillator which is synchronized with vertical sync pulses (pin 34). It forms a ramp voltage , which is used to control the vertical output stage. This same ramp voltage is used to form the adjusting signals for the image geometry using multipliers and sum circuits. When forming the ramp voltage, the circuits external components are the integrating capacitor at pin 27 and level adjusting capacitor at pin 25. This capacitor is used to keep the ramp amplitude constant whatever the frequency is. The ramp is extracted from pin 30. The ramp amplitude can be adjusted with the attenuator, whose attenuation is adjusted through the DC-voltage at pin 31.

The vertical ramp S-correction and C-correction can be adjusted with the DC-voltage of pins 28 and 29. If the ramp would be completely linear, the center of the picture would be squeezed compared to the picture's upper and lower edge. By adding S-correction to the ramp, the image becomes linear. Additionally, in some vertical output stages, a linearity error can arise, at which time the picture's upper half is not equal compared to the lower half. This error can be corrected with C-correction.

Also the geometry correction signals are formed from the ramp signal of the ramp generator. The E/W parabola is formed from the vertical ramp with the analogy multiplier and the attenuator. The vertical ramp is brought to pin 37 (E/W OUT) through the multiplier and the adder. The attenuation of the attenuator can be adjusted DC-voltage at pin 39, so that when the adjusting voltage is 2V, the attenuation is high and the parabola amplitude close to zero. Equally, if the adjusting voltage is 6V, the attenuation is low and the parabola amplitude approx. 3V.

The trapezium correction voltage is formed from the vertical ramp with the attenuator. The attenuator's attenuation can be adjusted with pin 38 DC-voltage so that when the adjusting voltage is 4V, the attenuator's attenuation is high and the output voltage zero. When the adjusting voltage is 6V, the attenuation is low and the output voltage high. If the adjusting voltage is 2V, the attenuation is also low, but the output signal polarity has been inverted to negative, so that the ramp coming from the attenuator is the inverted compared to the in going ramp. After the attenuator, the correction signal is directed through the adder to pin 37. The sum signal of the parabola and the ramp which is used to modulate the image width is thereby obtained from pin 37.

The orthogonal correction voltage is made with the same principle as the trapezium correction voltage. Its amplitude is adjustable with the pin 41 DC-voltage. The signal is directed to pin 41 through the adder.

The E/W balance correction voltage is formed from the vertical ramp with the multiplier and the attenuator. The multiplier transforms the ramp to a parabola which is then brought to pin 40 through the attenuator and the adder. The attenuator's attenuation can be adjusted with the DC-voltage of pin 42. The sum of trapezium correction voltage and E/W balance correction voltage is thereby obtained from pin 40, and is used to modulate the line deflection phase.

The control parabola for the vertical dynamic focus is obtained from the E/W parabola, which is switched to pin 1. The dynamic focus amplitude is not DC adjustable, but only the image height (the amplitude of the vertical ramp) transforms the amplitude of the dynamic focus.

The analogy multiplier contains also a DC-voltage input, pin 35. By changing the voltage of this pin (3.2…3.8V), an asymmetry to the geometry correction signals is obtained compared to the vertical sweep. If the pin is connected to the same voltage, which affects the vertical framing, the vertical lines of the image can be forced to remain vertical when shifting the image in vertical.

5.2.3. The protection functions

Protection functions have been added to the circuit in order to ensure the stable function of the external connections and the protection of the picture tube.

These functions are:

1. The cutting off of the line deflection output stages control signal (H OUTPUT INHIBITATION)

Is activated:

- If the supply voltage is under the internal reference of 7.5V
- If the XRAY pin 16 voltage is exceeds 8V
- If the H-duty pin 4 voltage is under 1V
- During the fly-back pulse. This is used to prevent the line deflection output stage transistor from going leading during the fly-back pulse.

2. The cutting off of the control signal (V OUTPUT INHIBITATION)

Is activated if :

- The supply voltage is under the internal reference of 7.5V
- The H-duty pin 4 voltage is under 1V

3. The blanking (composite blanking)

Is activated if:

- The supply voltage is under the internal reference of 7.5V
- The XRAY pin 16 voltage is over 8V
- The H-duty pin 4 voltage is under 1V
- During the line fly-back pulse
- During the vertical fly-back pulse
- During the field sync pulse

5.3 Function in practical switching

5.3.1 The supply voltage

The circuit 12V supply voltage is brought to pin 18. R222 and C215, C216 function as filtering components. The circuit forms reference voltages Vref and Href, which have their own filtering capacitors C226, C227 and C208, C209. The value of these voltages is approx. 8V. The ground of the circuit is pin 19. Additionally, the circuit has grounds Hgnd for the grounding of the horizontal block and Vgnd for the grounding of the vertical block.

5.3.2 The synchronizing

Vertical sync pulses are brought from the processors (IC501) pin 26 to pin 34 of the deflection driver circuit. Even if the circuit is operational and not dependent on the sync pulse polarity, the polarity is made constant positive in the processor. The value of C225 alone defines the frequency range of the vertical oscillator. In this monitor, C225 has been adjusted so that the circuit synchronizes itself automatically to the whole frequency range of the monitor (50…120Hz). If there are no sync pulses, the vertical deflection transfers to free oscillation frequency, which is approx. 100 Hz.

The horizontal sync pulses are brought to from the processor's pin 30 to pin 17. The polarity of the horizontal sync pulses is also made constant positive in the processor. The VCO of the circuit has been measured in such a way that the circuit synchronizes itself automatically to the whole frequency range of the monitor (30…72 kHz). C212 and R205, R206 together define the VCO frequency. With component values of the switching, the free oscillation frequency of the VCO is approx. 27 kHz and the maximum

frequency approx. 100 kHz. If there are no sync pulses, the horizontal deflection shifts to the free oscillation frequency. C210 and C211 are filtering components of VCO's internal circuits.

The frequency's feed-back is brought from the horizontal deflection output to pin 5 with resistor R221. Pin 5 is the current input, so that the pin has a transistor base, which has a protection resistor, so that the maximum pulse at the pin is only approx. 1 Vpp.

One should take in account that the circuit cannot function alone with a composite sync, because the circuit does not contain a separator circuit for the field sync pulses, and the phase/frequency comparator in the circuit is sensitive to possible additional sync pulses. The circuit is functional with composite syncs when the separation of field sync pulses is done before the circuit, in this case in the processor, and when the functioning of the phase/frequency comparator is prevented during the field sync pulse. The field sync pulse is brought to pin 14 through resistor R234.

5.3.3 The forced control of maximum/minimum frequency

To prevent the damage of the line deflection output stage due to a high frequency, it is necessary to prevent the maximum frequency of the H_Drive signal. Because the sync pulses arrive to the deflection driver through the processor, the maximum frequency lockout is done in the processor. If the horizontal frequency is too high (exceeding 72.5 kHz), it is prevented from leaving the processor. Thereby, even if the video card would deliver a too high frequency, the line output stage would not be damaged.

The minimum frequency of the H_Drive signal is also limited according to the switched S-capacitors. This procedure is meant to prevent the monitor horizontal deflection from operating in too low S-capacitor compared to the frequency. If the S-capacitors are too small, the AC-voltage inside them would rise too high, and the horizontal deflection output stage could be damaged. This kind of situation might arise for instance when changing the monitor "mode".

The lockout circuit has been built in the following way: a supposed situation where the horizontal deflection frequency is dropping and the AC-voltage in the S-capacitors starts to grow (C421). When the negative peaks are under 12V, the transistor gets base voltage through diode D421 and resistor R208 (F_LIMIT). T202 starts to lead and its voltage is simultaneously rising at its collector. At the same time, the VCO control voltage tends to rise through diode D201. At that time, the frequency drop stops and the circuit continues to operate at a frequency where the negative peaks of the S-capacitors AC-voltage are approx. 12V. The situation is stable until additional S-capacitors are switched on. At that time, the AC-voltage in the capacitors decreases, transistor T202 stops conducting and the frequency may to drop in the desired level.

5.3.4 The H-Drive output

An H-Drive signal is coming out from pin 21, and this is used to control the driver transistor T406 of the horizontal deflection output stage through buffer stage T422 and T423. The same signal is used to synchronize the width modulator IC401. Because the pin 21 output is of the open collector type, pull-up resistor R223 is needed.

The H-Drive signal pulse ratio is formed with the pin 4 voltage. Resistors R219 and R220 adjust the voltage to approx. 4.8V, at which time the pulse ratio is approx. 50%.

The information about the high voltage is brought to pin 16 from the high voltage generator. If the high voltage rises too high for some reason, pin 16 voltage goes over 8V and the IC prevents the forming of the H-Drive signal, at which time the horizontal deflection and the high voltage generator are shut down. The IC does not restart until the monitor has been restarted with the power switch.

5.3.5 The phase adjustment

The phase adjustment is realized with two phase locks one after another: PLL1 and PLL2. These two phase locks are used to adjust the picture position horizontally, PLL1 is used to adjust the picture and PLL2 to compensate possible temperature drift.

The user phase adjustment is done by changing the DC-voltage of pin 15. The adjustment voltage is brought to pin 15 through resistor R214 from the processor's D/A transformer pin 24 (H_POS). C202

functions as a filtering component. This DC- voltage defines the part of the VCO saw tooth wave (measurable from pin 10), where the line sync pulses are compared.

When the DC-voltage changes, the comparison point position changes also, at which time the saw tooth wave and the H-Drive signal move to another position compared to the sync pulse. The user can see this as a picture shift on the monitor screen to the right or left depending on the adjustment direction.

The circuit has been designed in such a way that when the adjustment voltage is at the half way (4V), the middle of the fly-back pulse is 12.5% from the phase time behind the front edge of the sync pulse. The whole adjustment range (2…6V in pin 15) is +- 12.5%.

5.3.6 The comportment when changing frequency

When the monitor deflection frequencies are changing (mode change), it is necessary to blank the picture tube. The mode change looks much better when no fuzzy flashes are distinguished on the screen. On the other hand, the stable function of the horizontal deflection output stage can be improved if the picture width is decreased before the mode change. The picture blanking must be fast, but also long enough, so that the new mode has time to settle before the image is restored.

Information is brought from the circuit's pin 2 if the phase lock is locked to the incoming sync pulses. During the frequency shifts pin 2 goes down, at which time transistor T206 does not get any base current from D204, and it goes non-conducting. This causes the screen blanking to activate through the G1 line, the G1 grid goes negative and the screen goes blank. Simultaneously, MUTE line goes down through resistor R225 and capacitor C405 discharges itself. The MUTE line affects the image width through width modulator IC401. When the line is down, diode 401 pulls down transistor T401's base and the image is decreasing in width.

When the phase lock has locked to a new frequency, pin 2 goes to high impedance mode (open collector) and capacitor C405 starts to charge through R224 and R225. At that time the image width starts to increase to the normal level at the same rate as the charge. The screen blanking is also interrupted. The image is not yet restored since the processor has adjusted the contrast and brightness settings to minimum during the frequency shift. The image is restored only when the processor restores the contrast and brightness settings to normal. The processor blanking period (approx. 0.6 s.) has been chosen is such a way that the new settings of the new mode have had time to stabilize themselves before restoring the image.

5.3.7 The vertical deflection control

5.3.7.1 The picture height

The control voltage V_AMP for the picture height is brought from the processor to the circuit pin 31 through resistor R253. The pull-up R256 adjusts the processor control voltage range 0…5V appropriate to the circuits control voltage range 2…6V. C224 functions as the filtering component. The control voltage in pin 31 transforms the vertical ramp amplitude coming from pin 30. The ramp wave controls vertical output stage IC203 through resistor R271, which is switched to the reversing input pin 7 of the output stage. The ramp's amplitude defines the current intensity, that is, the picture height, coming from the vertical output stages pin 5.
The picture is made linear with help of the pin 28 S-correction and pin 29 C-correction voltage. The S-correction voltage adjusts the vertical linearity between the image middle and lower/higher part. The C-correction voltage adjusts the vertical linearity between the higher and lower part of the image.

5.3.7.2 The vertical centering

The vertical centering control voltage V_POS is brought to pin 33. This control voltage is used to change the pin 32 VDCout DC voltage in the range 3.2…3.8V. This voltage defines the output stages non-inverting input pin 1 DC-voltage level through resistor R270. The DC level has been adjusted with resistor R272. When the VDCout DC-voltage differs from the 30 Vout solid 3.5V DC-voltage, the DC-voltage levels of the vertical output stage's pins 1 and 7 are not equal, which means that a DC-current component is created in the vertical output stages control. At that time, DC-current is flowing from the output stages pin 5 to the deflection coil or vice versa. Due to this, DC-current is flowing through the vertical deflection coil, that is, the picture location shifts vertically to the desired direction.

When changing the vertical centering, also the amplitude of geometry correction voltages must be altered, because otherwise the vertical lines will not remain straight when shifting the picture vertically. The needed adjustment is done by switching the voltage information of pin 32 to pin 25 (VDCin).

5.3.8 The geometry adjustments

5.3.8.1 E/W and trapezium adjustments

The E/W and trapezium correction voltages are combined in the processor. This is practical since both control voltages alter the image width, that is, the control voltages modulate the control voltage of the image width. The E/W -trapezium sum signal, the sum of the parabola and the ramp, is brought from pin 37. It is connected along the E/W line to the width modulator through R452. The parabola of the correction voltage is upwards and its base is locked to 2.5V. The parabola amplitude is adjusted approx. within the range of 0…2.9V. The ramp amplitude is adjusted within approx. +- 1V.

The control voltages similar to the correction voltages are brought from the processor to the circuit's pins 38 and 39 along E/W_AMP and TRAPEZ lines. Additionally, there is a feed-back from the E/W-trapezium output pin 37 to the E/W control voltage through the resistor R239. This is used to adjust the E/W correction parabola to the correct shape, so that the picture corners would be straight and of the correct shape.

5.3.8.2 E/W balance and orthogonality

The correction voltages of the E/W balance and orthogonality affect in a similar way the phase adjustment, as the E/W and trapezium correction voltages the picture width. The correction voltages have been former in a similar fashion. The output voltage at the circuit's pin 40 is the sum of the parabola and the ramp. The parabola base is locked to approx. 4V and its amplitude is of maximum +-4.5V. The ramp amplitude is maximum +-12% of the parabola amplitude.

The signal used for the correction is directed from the circuits pin 40 to phase adjustment pin 15 through resistor R218. The correction signal modulates the phase adjustment voltage and alters the time ratio between the VCO-ramp wave and the sync pulse. This can be seen on the screen as a phase shift in the rhythm of the correction signal. There is no changes in the frame.

The control voltages similar to the corrections are brought from the processor along the E/W_BAL line to pin 42 and the ORTHOG line to pin 41.

6 The width control circuit

6.1 General

The width control circuit is composed of pulse width modulator IC401, switch mode FET T405 and input coil M404. The pulse width modulator does not operate at the line frequency but at double line frequency. With this feature, there is the advantage that the input shock coil inductance can be low, and the circuit reacts rapidly to width changes. By this procedure, for example the trapezium correction is functioning without curves in the upper edge of the frame.

6.2 Function

The monostabile gets its triggering pulse from the edges of deflection driver IC201's pin 21 driver pulse. The rising pulse's edge is transferred through D406 to IC401 pin 11 without a delay. The pulse is connected to the IC's pin 12 through a small delay (approx. 500 nS), which is formed of R416 and C406. When the pin 12 voltage goes up (pin 11 is already up), the monostabile is trigged and pin 9 goes down at once. This voltage drives the FET T405 leading through buffer T402, T403 and capacitor C408. The current starts to flow to the S-capacitor C421 through T405 and M404. Simultaneously, the monostabile's capacitor C403 starts to charge and when its voltage has increased to the decision level, voltage at the pin 9 goes up. At that time, also T405 goes non-conducting, but since the coil M404's current cannot drop at once, the current starts to flow from M404 to the S-capacitor and back through diode D404 (Free-wheel diode).
After a while the driver pulse goes down, at which time the falling edge is connected through D405 to IC401's pin 12 without a delay. The IC pin 11 pulse connects after a small delay (approx. 500 nS), which is formed of R416 and C407. When pin 11 voltage goes up (pin 12 is already up), the IC's pin 9 goes immediately down. This results to the same function as with the positive part of the driver pulse, and the line output stage gets more supply electricity. This must happen before the current through D404 to input coil M404 stops, otherwise the regulation will not function properly. This is possible due to the proper dimensioning of the input coil which must have correct ratio compared to the pulse width.
The pulse width of the pulse width modulator (period when T405 is leading) will not change according the frequency. Because the pulse ratio will still increase at the same rate as the frequency (because the period T405 is non-conducting decreases at the same rate), the picture width will stay constant while the frequency increases.

6.3 Width adjustment and E/W-trapezium correction

The image width is adjusted by altering the charging time of capacitor C403, that is, the pulse ratio of the pulse width modulator. Trimmer RT401 is used to adjust the basic setting of the image width, that is, compensation of the variations in component tolerances. This way, the maximum picture width limiting in worst situations is reliable, and at the same time the whole adjustment voltage range of the processor's D/A transformer may be used.
The actual width adjustment comes from the processor through the resistor R453 on the WIDTH line. This voltage adjusts the T401 leading properties, which alters the current intensity to C403 and simultaneously the pulse ratio and image width. A high voltage (5V) in the WIDTH line results a narrow image.
The E/W and trapezium correction is done by summing the parabola and trapezium correction voltages to the width adjustment voltage through resistor R452.
The forced picture narrowing during mode change situations is done with the MUTE line and diode D401. When the frequency changes, pin 2 of deflection driver IC201 goes down, at which time the MUTE line goes down as well. The MUTE line pulls T401 non conducting through D401, at which time C403 charges faster, the pulse ratio decreases, and the image is narrowed. The return from this mode occurs slowly since T401 base goes up slowly while C405 is recharging.

When returning from a Start and Power Save mode, the picture is also narrow as the UVLO line discharges the capacitor C405 with diode D43 and the image gains width slowly with the time constant of R434 and C405.

6.4 The current lockout

The current used by the line output stage flows through resistor R411. The transistor T404 base has constant voltage realized with the help of D403, R413 and R412. If the line output stage current rises too high for instance when switching on the monitor, transistor T404's emitter voltage falls so low that T404 goes non conducting. Following this, T404's collector and pin 13 of pulse width modulator IC401 go down. Pin 13 is the Clear pin of the monostabile, which forces the monostabile's pin 9 to the static high position. The pulse width modulator does not give control pulses to T405 and accordingly does not give supply voltage to the line output stage. If the short circuit has not been eliminated during the next line sync, the function is repeated. This way, the circuit is protecting the power supply and the other circuits in a failure situation of the line output stage.

When repairing the line output stage, also the current lockout components and functioning must be checked. Special attention must be given to T405, D404, M404, M403, R410, R411, DZ401, R159 and R160. These components might be damaged when the line output stage is damaged, even if they seem to look undamaged.

7 The high voltage generator

7.1 General

The high voltage is composed of high voltage transformer M301, and the fly-back type voltage regulated power supply composed of transistors T304, T303 and IC301. The high voltage transformer contains in addition to the primary coils, secondary coils and secondary diodes, a high voltage capacitor and a Bleeder resistor. The trimmers for the adjusting of the focus- and G2-voltage are located in the Focus-pack (FOC301). Additionally, the transformer provides an OVER VOLT-voltage (M301, pin 2) which prevents the high voltage from rising too high, and a TCO-compensating pulse (M301, pin 3), which decreases the electric field emitted by the monitor. The feed-back data for the regulation of the high voltage is brought from the lower base of the Bleeder resistor (M301, pin 4) with the voltage formed in resistors R323, R322 and RT301. The trimmer RT301 is used to adjust the high voltage to 26 kV.

7.2 Function

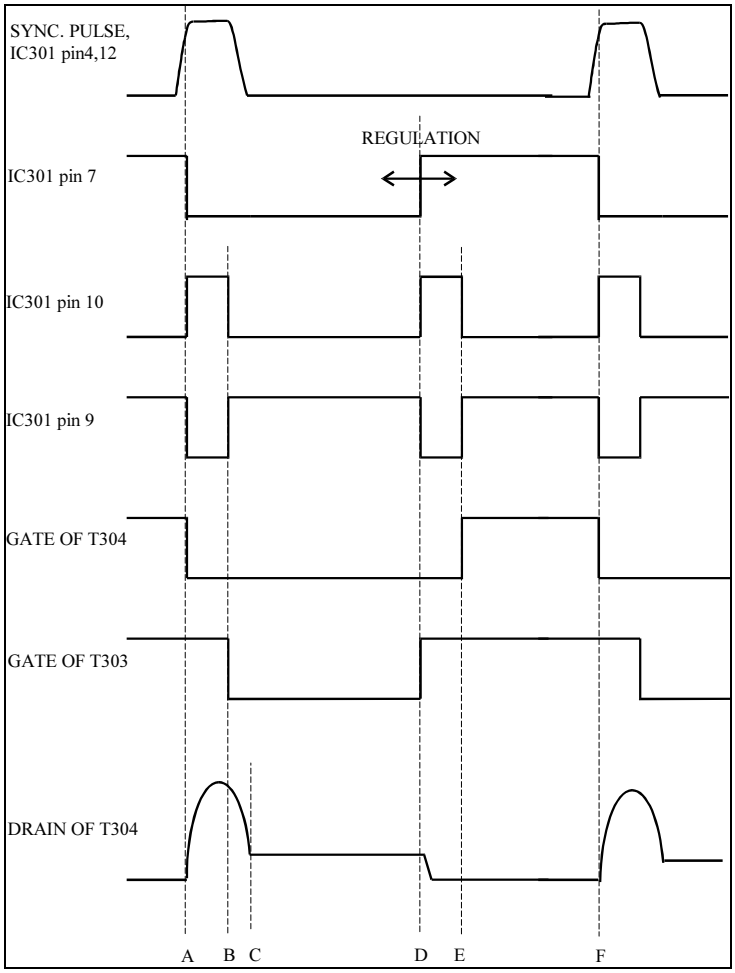
See picture 4

The functioning of the high voltage generator can be compared to the functioning of the monitor power supply, since the function principle is very similar (fly back-power supply) and same switching elements are found in the circuit. The primary coils (pins 9 and 10) upper end has a 160V voltage and switch mode switch T304 is located in the lower end. When T304 is leading, the current flows through the primary coil, at which time energy is charging to the high voltage transformer, similarly to the power supply functioning. When T304 is directed non-leading (part A), a fly-back pulse is generated in the T304 drain (time period A…C in the picture). The secondary diodes of the high voltage transformer start to lead and the energy charged in the primary shifts to the capacitance of the high voltage transformer and picture tube.

Since the coupling factor between the high voltage transformers primary and secondary is small (unlike in the power supply transformer), the drain voltage of the switch mode [switch] is not cut off like in the power supply, but ringing oscillations are easily generated in the drain. The capacitor C307 has been added to the drain to limit the maximum voltage and frequency of the ringing.

Different than in the power supply, the T304 drain has a large capacitor (C307), and it is important that this capacitor is discharged before switch mode switch T304 is again driven to conduct. Otherwise the capacitor would discharge through the switch mode switch which would get overheated. On the other hand, the drain ringing after the fly-back pulse must be eliminated, so that the voltage regulation would function properly. This has been realized with switch T303. Just before the end of the fly-back pulse (period B), switch T303 is directed leading. At that time, after the fly-back pulse, the current flowing in the primary coil from pin 10 to pin 9 remains in a loop: primary coil…T303…D306. This starts in the stage where capacitor C307 has discharged just under 160V and diode D306 turns forward (period C). This goes on as long as T303 is leading and T304 non-leading (time period C…D). Just before T304 is driven

to conduct, T303 is drive non-conducting (period D). At that time, the current flowing in the primary coil has been forced to follow the following route: primary coil, 160V capacitors (C141, C142)…C307, and C307 starts to discharge. When C307 has been completely discharged, instead of C307, the current flows through a diode inside T304 not shown on the picture (time period D…E). At this point T304 can be driven conducting (period E). Since the primary coils voltage is now over 160V, the current in the coil turns fast and starts to flow to the opposite direction from pin 9 to pin 10 and so on to the ground of T304, energy is charged to the coil and so on, and the cycle starts from the beginning.



Picture 4

7.3 The SJ-driver

The correctly timed control of the switch transistors is done by monostabile IC301 which is realized with the 4538 circuit. The circuit contains two identical monostabiles, whose time constants are defined with external components.

The rising edge of the sync pulse for pins 4 and 12 triggers both monostabiles A and B (A= pins 1-7; B= pins 9-15) at time A. At that time, monostabile A's pin 7 (inverted output) goes down and pulls transistor T304's grid down with transistor T306. T304 goes non-conducting and the high voltage fly-back pulse begins.
T303 is still non-conducting. After a period defined by the time constant R301, C302, the monostabile B changes its mode and its output pin 10 goes down. The time constant in picture 7 corresponds the time period A…B. Since pin 7 voltage is down, the transistor T303 grid is driven down with resistor R304 and transistor T302, and T303 becomes conducting.

At the moment defined by the high voltage regulation, monostabile A reaches its decision level (period D in the picture), output pin 7 goes up and the inverted output pin 6 goes down. Transistor T303's grid goes up with the help of resistor R304 and transistor T301, and T303 goes non-conducting.

The change in pin 6 triggers monostabile B, which changes its mode. Pin 9 goes down, thereby preventing transistor T304's grid from going up through resistor R303. After a period defined by time constant R301, C302 (point E in the picture), monostabile B's pulse ends and pin 9 goes up. T304's grid is free to go up and T304 is driven to conduct. At that time, energy starts to charge in the high voltage transformer's primary coil. At the moment F, a new trigger pulse is brought, T304 goes non-conducting, the fly-back-pulse begins, and the energy charged in the primary is transferred into the secondary and so on.

7.4 The regulation

Unlike the power supply (current mode regulation), the high voltage stage's regulation uses voltage mode, that is, the pulse ratio of the switch mode switch is changed according to the fee-back information brought from the secondary. The longer the leading time of switch mode switch T304 is, the longer the primary current is and the larger the energy amount transferred to the secondary is, which means more charge capacity from the secondary.

We examine the situation through an example: if the beam current increases, the high voltage tends to decrease. Following this, the C311 voltage in the lower end of the Bleeder resistor tends to decrease. This means that also the voltage in pin 9 of high voltage differential amplifier IC304 tends to decrease. The IC's pin 10 has a reference voltage (approx. 6V), against which the feed back information is compared. Consequently, IC304 pin 8 voltage rises, at which time IC301 monostabile's capacitor C301's charging takes less time. In the previous picture this means the shifting of period D to the left, that is, T304's grid's down position period, and simultaneously, T304's non-conducting time decreases. This results that when T304's grid goes up at the moment E and T304 starts conducting, it has time to lead for a longer period of time before the new trigger pulse arrives at point F. Triggering pulses are brought in line frequency, so that the period between A and F is constant. Since T304 leads for longer period of time, more energy is charged to the primary coil of the high voltage transformer, at which time T304 goes again non-conducting, more energy is charged to the secondary coil, and the high voltage increases back to the desired level.

7.5 The current limiting

The current limiting of the high voltage generator is realized with transistors T307 and T306. The current limiting protects the generator for instance in a start-up situation, where the generator tends to bring a maximum of current to the secondary. The current limiting is also needed in failure situations.
If the high voltage generator's current rises too high, the R324 voltage rises so high that T307 starts to conducts, at which time also T306 starts to conduct. This holds T307 conducting; the circuit functions as a thyristor. Since the transistors are conducting, the transistor T304's grid goes to the ground, and the current going through the high voltage transformers primary coil is stopped. Transistors T307 and T306 remain conducting as long as T305 conducts. When the control from IC301 to T305 is interrupted, T307 and T306 go non-conducting as well, since the hold current for their control is interrupted. When IC301 gives the next pulse for T304, the function is repeated if the over current situation has not finished.
When repairing the high voltage stage, it is always important to control also the components and function of the current limiting. Special attention must be given to the function of T304, T303, D306, T305, T306, T307, R318, R317, R316, R3314, R315, C308, R159 and R160. These components may be damaged during the failure of the high voltage stage, even if they seem undamaged.

7.6 Start-up situation

To ensure the proper functioning during the start-up moment, the operating of the high voltage stage is prevented when the supply voltages are too low. This is done with help of the UVLO signal. When the voltages are too low, the UVLO signal is down, so the T306 base is down as well. At that time, if T305 is conducting, T306 is conducting as well, and the high voltage switch T304's grid remains down, so it does not conduct. This prevents possible failure situations when starting up, and the high voltage stage is not damaged. When the supply voltages have increased to the right level, the UVLO signal goes up, so that the high voltage stage can start normally.

7.7 The G2-voltage generation stage

The G2 voltage needed by the picture tube is brought from the trimmer in the Focus pack. A G2 voltage fine tuning possibility has been added to the circuit for production reasons. The idea of the fine tuning is to change the Focus pack lower end voltage, at which time the G2 voltage brought from the trimmer is

changed as well. The focus voltage is changed simultaneously, but the proportional change is so small that it can be ignored.

The voltage is adjusted with the circuit composed of transistor T311 and resistors R385, R333. T311's base is in a constant voltage (approx. 5.5V) composed with R335 and R387. If the processor G2_ADJ-DAC (DAC14) voltage is high (approx. 5V), T311 does not lead, and current is not going through it. At that time, the voltage of the Focus pack's lower end (Q301 pin 1) is defined by resistor division in the Focus pack, R385, R333. The total resistance of the Focus pack is approx. 80 Mohm, so Q301's pin 1 voltage is approx. 240V. If the processors G2_ADJ-DAC (DAC14) voltage is down (approx. 0V), T311 is conducting, at which time its collector has a voltage of approx. 5V. At that time, a current of approx. 140 uA is going through R390, T311 and R385. The voltage of the Focus-pack's lower end (Q301 pin 1) is approx. 65V in that point. The fine tuning voltage of G2 is approx. 175V, which is enough for the needs of production procedure.

7.8 X-ray protection

A pulse relational to the high voltage is brought from the high voltage transformer's pin 2, which is used to prevent the x-ray generating in a situation where high voltage tends to increase too much. The pulse is transformed to DC-voltage with diode D305 and capacitor C304. This voltage is decreased to the right level and connected with R306, R307 and R308 to the deflection driver IC201's x-ray-in pin 16. If this pin's voltage increases over 8V, the circuit interrupts the driver pulse feed to the line output stage. Since the high voltage generator gets a trigger pulse with a line fly-back pulse brought from the line output stage, the high voltage generator is shut down as well. This prevents the high voltage from increasing too much. Since the deflection driver does not give a new driver pulse until its supply voltage has been interrupted for a moment, this situation requires the monitor to be shut down.

8. The vertical output stage

8.1 General

The used vertical output stage is a SGS-Thomson TDA9309 circuit. The circuit has an output amplifier, a fly-back pulse generator and a thermal protection circuit. The circuit operates with a double polarity supply voltage.

8.2 The function

The circuits positive supply voltage (approx. 16V) is brought to pin 2. The negative supply voltage (approx. -11V) is brought to pin 4. A ramp voltage is brought from the deflection driver, which is connected with resistor R271 to the circuits inverting input pin 7. The vertical centering is done with resistors R270 and R272 by changing the DC-voltage level of IC203's non-inverting input pin 1. The vertical deflection coil is connected to IC203's pin 5. A voltage comparable to the deflection current is brought from resistors R279 and R278, and is connected with resistor R277 to IC203's reversing input pin for the right protection.
The attenuation circuit R280, R281 and C233 is used to attenuate the oscillations generated during the vertical fly-back, which could be seen on the upper part of the screen as deflection non-linearity or fly-back lines. C234 is used to prevent the circuit oscillation in high frequencies. D207 is a diode needed by the fly-back pulse generator, and used to increase the fly-back pulse to a higher level and decrease the fly-back time.
A positive vertical fly-back pulse is brought from IC203's pin 3, with an amplitude of approx. 27V. The pins voltage is approx. -11V during the sweep and approx. 16V during the fly-back.
The protection circuit inside the vertical output stage protects the circuit from a short circuit and over heating situation.

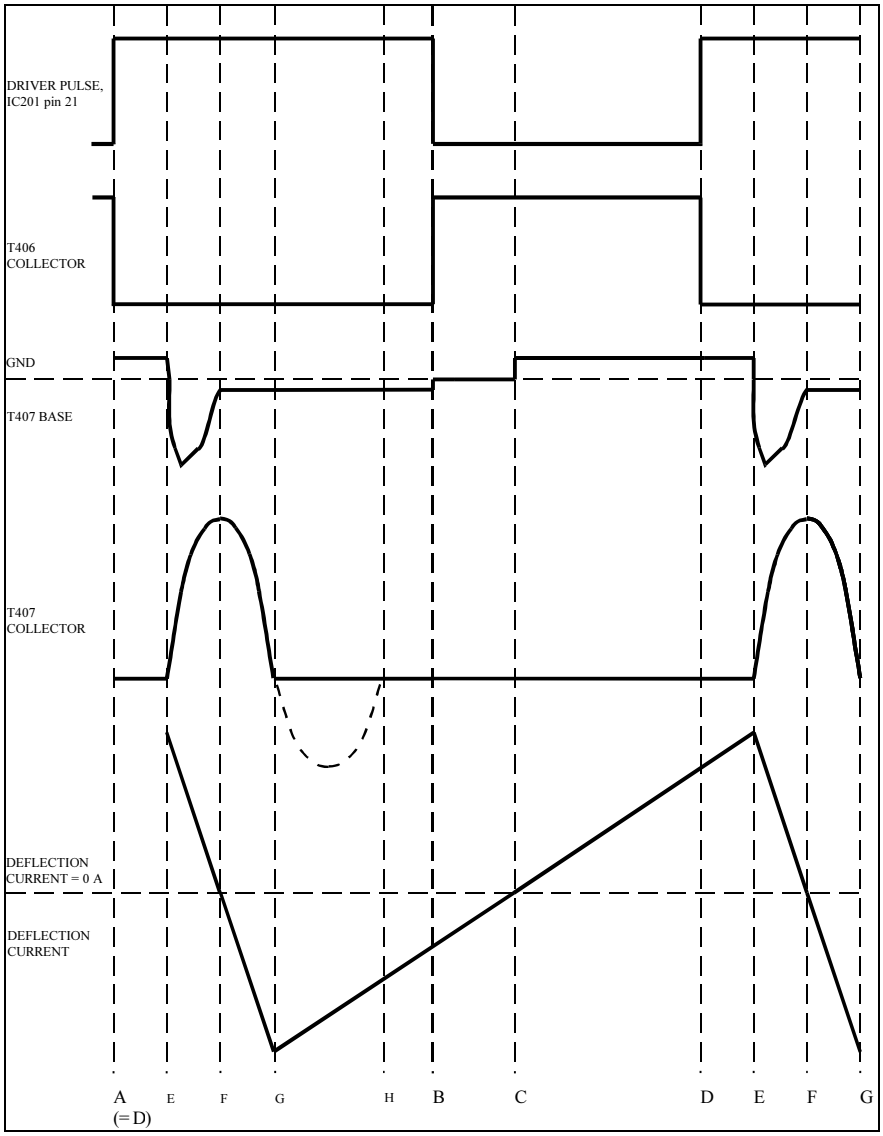
9 The line output stage

9.1 General features

The line output stage is composed of output transistor T407, fly-back diode D410, fly-back capacitors C413, C415 and driver transistor T406, its buffer circuit T422, T423 and driver transformer M401. Additionally, there is an S- and linearity-correction circuits, a frame centering circuit and a current lockout circuit.

9.2 The function

The function is shown in picture 5.



Picture 5

The line output stage gets a positive driver pulse (amplitude approx. 10V, rising edge) from deflection driver IC201 pin 20, point A in picture. This pulse makes the driver transistor T406 conduct, so that current is flowing in the primary side of driver transformer M401 (pins 7 and 9), and energy is charging into the transformer. Simultaneously, due to the coiling directions of M401, its pin 4 is down, so that T407 does not conduct (period A-B). When the driver pulse goes down (part B), T406 is blocked, and the current flowing through M401's primary is interrupted. At that time, the energy charged in the transformer discharges to its secondary and T407's base rises to approx. 0.7V (part C). T407 gets base current and starts to lead. Current starts to flow from S-capacitors through the deflection coil to T407. The increasing speed of the current depends of the inductance of the deflection coil and the amount of

voltage in the S-capacitors. The electron beam moves from the image center to the right edge, and energy is simultaneously charged to the deflection coil. M401 has been charged with so much energy in the previous phase that T407 is getting enough base current during the whole process time. When the driver pulse increases again (point D), T406 goes leading, at which time current starts to flow through M401's primary. Due to this, M401's secondary voltages polarity is changed and T407's base charge starts to discharge (time period D-E, so called storage time). When T407's base charge has been completely discharged (point E), its base goes very rapidly negative, so that its collector current is interrupted also very rapidly. The electron beam is at its extreme position to the right.
Since there is energy in the deflection coil and T407 is not leading, the oscillation circuit formed by the deflection coil and fly-back capacitor C413 (and C415, which is serial with the fly-back capacitor) starts to oscillate. Due to this, the energy in the deflection coil is transferred to the fly-back capacitor (period E-F). At that time, the fly-back capacitor voltage increases greatly to approx. 1000V (line fly-back pulse FBP). Simultaneously, the horizontal deflection direction in the picture tube reverses and the electron beam (which is blanked, so it will not be seen on the tube) will start to move very rapidly from right to left.
At the moment where energy starts to flow back from the fly-back capacitor to the deflection coil (point F), the deflection current is zero and the electron beam in the middle of the picture tube (still blanked, so it will not show on the tube).
When all the energy has flowed back from the fly-back generator to the deflection coil, the deflection current is in its negative maximum, and the electron beam in its extreme position to the left (part G). At that time, the oscillating circuit formed by the deflection coil and the fly-back capacitor will tend to continue to oscillate on the negative time period (period G-H), but this is prevented with fly-back diode D410. Since there is still energy in the deflection coil (and it cannot disappear by itself), the deflection current now starts to flow from the deflection coil through the S-capacitors to the ground and from there back to the deflection coil through the fly-back diode (period G-C). At that time, the electron beam deflects towards the picture tube center. When the energy in the deflection coil is zero, the beam is in the middle of the picture tube (part C). Before that moment, Driver transistor T406 has gone leading with a decreased driver pulse (part B). At that time, when the deflection current is zero, T407 starts to lead and the function begins from the beginning (part C). T407 will not start leading in part B, since current is flowing through the fly-back diode, and the transistor collector is negative compared to the emitter.

The capacitor C415 is used to produce an approx. 60V fly-back pulse for the horizontal clamping. D412 is a level clamp diode, used to lock the T415 period sweep voltage to the ground level.

9.3 Linearity correction

Since this monitor operates in a wide frequency range, a frequency dependent S- and linearity correction is needed in the horizontal deflection. For this purpose, there are interchangeable S-capacitors C426-C429, switch FETs T426-T430, linearity coil L403, its parallel coil L407 and switch FET T411 in the line output stage.
The processor chooses according to the used horizontal deflection frequency a proper combination from the S-capacitor table and directs the appropriate switch FETs to conduct through lines S0…S4. The principle is: the lower the line frequency is, the more capacitors are connected.

The linearity correction is done with linearity coil L403. Since its correction influence is too high for higher frequencies, the parallel coil L407 is switched into the circuit. This is done by pulling down processor pin 16 (LIN), at which time T413 is blocked and switch FET T411 starts to conduct.

R426 and D414 remove the oscillations generated in the linearity coil. D423 and C438 are used to make a positive grid control voltage for T411. DZ403 limits the generated voltage to 12V.

9.4 Frame centering

The frame centering is done with transformer M402. Since the current needed by the line output stage is fed through M404 to the S-capacitors, DC-voltage is flowing through the deflection coil to transistor T407. When flowing through the deflection coil, the current causes frame shifting to the right. For this reason and because of the tube/deflection coil tolerances, the frame centering need is generally higher on the left than on the right. Centering transformer M402 is connected parallel with the deflection coil. DC-current is being generated to coils 3…5, if the impedance seen by the current is different when the current flows from pin 3 to pin 5 than from pin 5 to pin 3.

If the processor drives the H_CENT line down, transistor connection T409, T421 is non-conducting, and current can flow only to one direction through diodes D419, D420. The transformer's DC-current is now at its maximum and it over-rides also the DC-current going through the deflection coil, and thereby shifts the frame to the left.
When the H_CENT line voltage is being increased, transistors T409, T421 start to open slowly. Current can now flow to the other direction as well, at which point the DC-current going through the transformer decreases and the frame moves to the right. When the H_CENT line voltage is 5V, transistors T409, T421 conduct freely, and the current going through them is a bit higher than the current through the diodes D419, D420, at which point the frame has moved to its extreme position to the right.

10 The blanking circuit

10.1 The line blanking

The line blanking is done with video pre-amplifier (ICH1). The line blanking pulse (H-BLANK) is made from the line fly-back pulse with port IC502 B (NOR-circuit). The image is blanked when IC502's pin 5 or 6 is up. The pulse is directed from here to the video pre-amplifier's pin 13. The negative pulse in pin 13 drives the output voltages of the pre-amplifier to zero V. At that point, the voltage of the output amplifiers output and the cathodes increases approx. 10V. This causes the beam to be blanked during the fly-back.
The line blanking pulse's leading edge is obtained current controlled with C445 and R455. Part of the fly-back capacitor C413's current is directed through capacitor C445 and resistor R455, at which point the voltage over R455 increases rapidly as soon as the fly-back pulse begins. This voltage (H_BLANK_STR) is directed to IC502's pin 5 through resistor R526. This prevents the generating of a bright red vertical stripe in the right edge of the frame.
The blanking of the sweep period is done with a fly-back pulse (H_FLY) brought to IC502's pin 6 through resistor division R456, R457. The blanking length of the left edge is defined by the ratio of resistor division R456, R457.

10.2 The vertical blanking

The vertical fly-back blanking is done with the G1 grid of the picture tube. The grid's voltage is dropped negative to approx. 70V during the vertical fly-back, at which point the beam is blanked.
The blanking pulse is brought from transistor T206, and directed to the base board, phase lock and G1 grid.

A positive vertical blanking pulse is brought from pin 3 of the vertical output stage, and conducted to processor (IC501) pin 20 (VFBACK) through resistor division R237, R202. Diode D209 is used to prevent the forwarding of the approx. -11V negative pulse of the vertical output stage pin 3 during the sweep period, since the processor cannot handle it. The fly-back time is adjusted to 350-400 uS with C236. This makes sure that there are none or rare bright lines in the image upper edge. A negative vertical blanking pulse (V_BLANK) is brought from the processor pin 36, to which is summed internally a vertical sync pulse from pin 26 and a fly-back pulse from pin 20. The sync pulse is summed to prevent a short fly-back line part in the image lower edge. IC501's pin 49 (HFBACK) is connected to ground, so the circuits line frequency blanking function is not operating. The processors pin 36 is an open collector type and has a pull-up resistor R518. The vertical blanking pulse is connected through transistor T206 along the G1 line to the base board where it activates the blanking circuit.

11. Other functions

11.1 The beam current limiter circuit

The beam current limiter circuit is composed of transistors T309 and T308. The beam current flows from ground through resistor R320 to pin 4 (lower end of the secondary) of the high voltage generator M301. When the beam current rises too high, T309 starts to lead. At that point, also T308 begins to lead and decreases the contrast and brightness control voltages along the BCL-line. Due to this, the beam current decreases. R326 is used to produce a small amount of bias-voltage to T309, at which time the beam current limiting changes due to temperature variations is prevented. The long time constant R319 and C309 keeps the lockout voltage constant during the whole field sweep. Since the brightness adjustment

voltage measurement is done in such a way that its DC level is higher than the DC level of the contrast adjustment voltage, the beam current limiter decreases first the brightness, through resistor R568 and diode D508. This procedure is meant to stabilize the contrast ratio whatever the image content.

11.2 The TCO compensating circuit

The compensating circuit produces voltages that are independent from the line frequency and the beam current to the wire loop in the picture tube mask, and which are reverse phased compared to the field coming from the picture tube. The voltage depending on the beam current is done by measuring the current of M301's high voltage capacitor with resistors R343, R322. The produced voltage is inverted and reinforced with an amplifier formed of T312…T315. The high voltage generators fly-back pulse (coil 7,3) is summed to this voltage, after which the voltage is summed to the line frequency compensating pulse in transformer M402 (Centering transformer, pins 9 and 7). Components C416, C417, C437, R420, RT402 and RT403 are used to shape the pulse, at which point the pulse form and phase are optimized to the pulse coming through the picture tube. The wire loop connected to connector Q402, which is connected to the mask, makes the electric field compensating, removing thereby the electric field arising from the picture tube and the deflection coil.

11.3 The reset circuit

The reset circuit is composed of T507, T506 and their auxiliary components. If the VXX-voltage (+5V) is too low (under 4.5V), T506's grid has a voltage under 2.5V and it does not conduct. At that time, T507 base is up, so it does not conduct either. R554 pulls down the processor Reset-pin (IC501 pin25), resulting in a reset situation.
When VXX (+5V) rises high enough (over 4.7V), T506's grid rises over 2.5V, at which point it goes conducting. At that point, T507 goes conducting as well, so the processor pin 25 goes up, and the processor is started-up. C529 and C530 are used to elongate the reset signal to the wanted level after the rise of the voltages.
In a cross-over situation, the processor often fails in its program execution. In this monitor, a protection circuit has been made to prevent these situations, which forces the processor to a reset-mode every time a cross-over occurs in the picture tube.
In a cross-over situation, there is also a high current going through high voltage transformers (M301) internal high voltage capacitor. Due to this, the capacitor's lower end voltage changes abruptly and the Glimmer lamp GL302 is lit. At that point, current is also going through R334, since the cross-over current tends to come back to the picture tube through connector W301 (FLASHOVER GND). A voltage loss therefore occurs over the resistor R334, which drives opto isolator IC302 to conduct. At that time, also its transistor is leading, pulling down the FO_RESET line. This line is connected to T506's grid through diode D516, so it is saturated and saturates T507 as well. As a result, R554 pulls down rapidly the processor's reset-line, so that the processor goes to reset mode for the duration of the cross-over situation. When the cross-over is over, opto isolator IC302 is also saturated, so that T506 grid goes up rapidly and the processor begins its operation from the start, ignoring possible failure situations during the cross-over.
GL304 protects resistor R334 from a too high voltage in a cross-over situation. DZ303 and R389 perform the same protection for the opto isolator. Resistor R527 is the pull-up needed by the opto isolator and C539 prevents disturbances from affecting the reset-circuit. R596 is used to produce hysteresis to the function of the reset circuit, so it will not remain oscillating, if VXX remains in the working point of T506 for a longer period of time.

11.4 The clamp pulse production

The black level clamp pulse needed by the video is produced from the horizontal sync pulse. Since the monitor does not have to be operating on a sync on green-synchronization, the clamp pulse can be produced directly from the sync pulse without additional circuits. A positive sync pulse is brought from the processor's pin 30 (H_SYNC), which is connected to IC502's pins 2 and 3. The negative inverted pulse needed by the video is brought from the circuits pin 1, and is connected through protector resistor R5561 to pin 15 of connector Q501 and there on to the video board.

11.5 The Moiré adjustment

The Moiré control is made with line driver (IC201 pin 23). The circuit outputs a square wave, with a frequency half of the frequency of the line frequency. Additionally, the square wave phase changes after

every field during the vertical deflection phase. The pin is an open collector, and the needed pull-up is realized with the processors DAC1 (IC501 pin 4). The Moiré control square wave is connected to R216 with R211. This resistor is in serial PLL2C (pin 3) with filtering capacitor C206. When resistor R216 voltage is changed, its image phase is also changed. This makes the image shift one period after another horizontally to the right and the left, so that the Moiré is removed; simultaneously, the vertical lines are thickening a bit (less Focus). The degree of the Moiré adjustment is defined by processor's pin 4 voltage, high voltage means higher Moiré correction. When correctly adjusted, the movement is less than one pixel, so it should be seen as decreasing Moiré and not affect much the thickness of the vertical lines (means lesser Focus).
The Moiré adjustment is timing mode dependent, since the Moiré in the picture is changing according to the resolution and the image height among others. This way, a Moiré setting value can be adjusted on every memory setting, and really optimized separately. With a new setting (non-optimized mode) the Moiré adjustment is been set to 0, at which time the Focus is always the best possible.

11.6 The demagnetization circuit

Magnetism is often remaining in the iron parts of the picture tube and the monitor, which can be decreased by generating a large attenuating magnetic field with AC-current. For this purpose, a demagnetization coil has been installed around the picture tube. The processor demagnetizes always when the monitor is started up. The user can also execute it by pressing the demagnetization button.

When the demagnetization begins, processor pin 15 goes up (to 5V) for approx. 1 second. At that point, C136 charges rapidly to approx. 5V voltage and T111 goes leading. T111 switches relay RE1 as pulling and the mains current starts to flow through the demagnetization coil. The PTC resistors (PTC1 and 2) connected serial with the demagnetization coil heat up rapidly, their resistance increases and the demagnetization current decreases, at which point the possible magnetism in the iron parts of the monitor is removed. C136 and R143 continue the pulling time of the relay for approx. 5 seconds, and when C136 voltage has been discharged through R143 so low that T111 goes non-leading, the relay lets go and switches off the demagnetization coil from the mains current, at which point also PTC1 and 2 lack the current and cool off, so that a new demagnetization procedure can be started after a while.
D121 is used to disconnect the processor pin from T111's grid when the processor pin is down but when C136 has not yet been discharged. R142 functions as a protection resistor and D141 function is to prevent the demagnetization when the monitor is shut-down.

12 DDC

12.1 General

Display Data Channel or DDC is a two-way data transfer channel between the monitor and the computer. It can be used to transfer for instance information about the computers properties, the highest refreshing frequency, so that the computer can take advantage of the whole performance range automatically. DDC is using the data and clock lines of the signal cable (SDA and SCL).

12.2 DDC levels

When the monitor is started and the processor gets the supply voltage of +5V, it starts to send a DDC1 level signal on the SDA line clocked by the field sync pulse VS. When the transmission has begun, the field sync pulse frequency can be increased up to 25 kHz. In this mode, the clock line SCL is up. DDC1 is thus one way data transfer to the computer. The processor shifts to DDC2B level when it notices a falling edge in its SCL input. DDC2B is a two-way data line, where the data transfer is based on the I2C standard. The computer can drive the processor to switch to the DDC highest level, known as DDC2AB.

12.3 DDC practical circuit

The monitor can communicate at DDC1, DDC2B and DDC2AB levels. The DDC line comes to the monitor's connector Q501 through the signal cable and the base board, and it is connected to the processor pins 51 (SCL1) and 52 (SDA1). The processor contains the EEPROM circuit and all the other functions needed by the DDC, so that not many external components are needed.
R547 and R528 are the pull up components of the DDC line. R571, R572 and D511…514 operate as protection components to external ESD or other disturbances.

13 Audio

13.1 The audio amplifier

The audio amplifier is a Philips made two-channel bridge coupled TDA7057 circuit. The circuit contains a stereo pre-amplifier, a bridge coupled stereo output amplifier and a thermal protection circuit.
The circuits supply voltage is connected to the circuit pin 4 through resistor R372. The capacitor C350 operates as the filtering capacitor of the supply voltage, at which point the supply voltage does not decrease during music high peaks, and enough temporary power can be obtained without any distortion.
The line level audio signal is connected to the RCA connectors Q308, Q309 in the back of the monitor, and from there on through resistors R377, R378 and coupling capacitors C353, C354 to the circuit's input pins 3 and 5. Resistors R357, R356 are used to decrease a bit the level of the incoming signal, at which point the whole volume adjustment range is obtained. Capacitors C355, C356 are used to limit the high limit frequency of the amplifier.
The volume adjustment voltage is connected from the processor (VOLUME line) through R383 to the amplifier's pins 1 and 7. The volume balance adjustment does not exist, but the volume affects both channels at the same time. R373 is used to decrease the processor 0-5V adjustment range to approx. 0.2V, since it is an adjustment range of the amplifier circuit. When the adjustment voltage is under 0.4V, the audio amplifier goes to a so called mute-mode, at which point its power consumption is small.
The speakers are connected to connector Q305 from output pins 8, 10 and 11, 13. Connector Q304 has an additional module, containing among others a headphone connector and a plug for an external microphone.
The sound signal goes through this module which is located at the side of the monitor, since the speakers must be disabled when using headphones. This is realized with the headphone plug contacts in the module, which are in short circuit when the headphones are not in use. At this point, pins 2 and 3 (4 and 5) of Q304 are in short circuit. Q304 pin 6 (ground) is the ground of the headphones, when using headphones the amplifier thus not operating as bridge coupled, at which time the obtained power is smaller as required for the headphone use.
The purpose of transistor circuit T317, T318 is to reduce the sound volume if the output stage power is rising too high. This occurs in a situation where the input signal on the RCA connectors is greater than the line level, for instance with some sound cards. In this situation, the current taken by the output stage increases, at which point resistor R372's voltage loss increases exceeding 0.7V. As a result, T317 goes leading and pulls up T318 base, thus reducing the volume adjustment control. C359 is used to prevent temporary music heights from affecting the sound volume. The circuit in question is operating only when much power is being taken from the output stage for a reasonable period of time.

13.2 The microphone amplifier

The microphone amplifier is a Philips made TDA1013 circuit. It is a DC adjustable single channel (mono) amplifier-IC which contains a DC adjustable pre-amplifier and output stage.
The amplifier supply voltage is connected through R361 to the amplifier. R3611 and C341 are used to attenuate the possible drops caused by the audio output stage to the supply voltage.
The microphone signal is connected with an additional module to connector Q310. The module has an external microphone plug which disconnects the internal microphone located in the upper part of the monitor.
T316 operates as the microphone pre-amplifier transistor. R366 and C344 are used to reduce the low limit frequency of the microphone amplifier. The amplified microphone signal is connected with capacitor C343 to the amplifier IC305 pin 8. The microphone amplifier amplifying can be adjusted with the processor through MIC_VOL line, which is connected to pin 7 of the microphone amplifier. The microphone amplifier's output level can be adjusted from mV level to line level (approx. 1 Vpp). R368 and C346 are used to connect the signal coming from IC305 pre-amplifier to its output amplifier. C347 is used to reduce the high limit frequency. The amplified signal is brought from pin 2, and the DC-voltage is removed from it with capacitor C349. Resistors R370, R371 are used to decrease the signal brought from MIC_OUT connector Q307 located behind the monitor, at which time possible noise etc. are attenuated. R369 and C348 are used to prevent the oscillations of the amplifier.

14 The processor

The used processor circuit (IC501) is a 8-bit SGS-Thomson ST7272 designed for monitor use. In addition to the normal processor functions, it contains also a block for the shaping of sync pulses, a DDC block and a IIC line driver to execute the DDC functions. It has also 16 10- and 2 12-bit DAC (Digital Analogue Converter) circuits for the control of DC adjustable circuits and 8 8-bit ADC (Analogue Digital Converter) circuits for the measuring of incoming DC-voltages. Additionally, it has also a block for the generating of a blanking signal and open collector circuits for instance for the control of S-correction FETs. There is no need for an external EEPROM circuit for the saving of setting values since the circuit in question is included in the processor. Since this internal EEPROM circuit has limited memory amount, there is a slot on the circuit board for an external EEPROM circuit (IC504), though not needed on the basic device.
In addition to these functions, also present on the circuit are a video black level clamp pulse generator and an E/W generator (EWPCC), not needed though since their function is not satisfactory enough.
The processor controls all the functions of the monitor according the line- and field frequency and the user settings.

14.1 The handling of sync pulses

The vertical sync pulses are connected as they are to processor pin 27 through resistor R531. The line sync pulses are connected through IC502 (C and D ports) to processor pin 29. R529 and C 537 are used to produce a small negative bias shift to the horizontal sync pulse, since IC502's decision level is under 1V. Without the circuit in question, the jitters would increase too much, since the sync pulse is generally clearly rounded near 0V, at which point the noise at the decision level easily produces jitters. Additionally, IC502 accelerates clearly the edges of the sync pulses, since processor jitters increases on slow pulses. R598 is used to produce some hysteresis for IC502, which in its turn reduces the jitters. R532, R530 are pull-up needed by the sync lines. D504 and D506 are used to prevent the voltage connection to VXX line(+5V) from the PC through sync pulses, since this might scramble the processor function in a situation where the monitor is not operating, but the signal cable is connected to the operational PC.
The processor accepts both sync pulse polarities and also the composite sync, at which point it isolates the vertical and horizontal sync pulses inside the processor. The constant positive vertical sync pulses come out from processor pin 26 and horizontal sync pulses from pin 30.
If the frequency limits are crossed (for instance horizontal sync pulses over 72.5 kHz frequency), or there are no incoming pulses, the processor generates the sync pulses, which happens, for instance, in a self-test situation.

14.2 The keypad reading

The processor reads the keypad located in the front of the monitor through AD-converters (pins 17-19). The keypad is connected to connector Q502. When no key is pressed, connector Q502's pins 10-19 are in the air. This means that processor pins 17, 18 have an approx. 5V voltage due to pull-up resistors R591 and R593. Since connector Q502 pin 3 is connected to the grounds internally in the keypad, the processor pin 19 has an approx. 4.1V voltage (voltage division R592/R582-584). This is interpreted by the processor that the keypad is in place and has not been pressed. If the processor pin 19 voltage rises to 5V, it means that the keypad is not in place (Q502 pin 3 is in the air), and the processor is blinking the led in this failure situation.
When the user presses some key, one of the Q502 pins 10-19 goes to ground, and due to the change in the resistor division the processor pins 17-19 voltage is altered and the processor detects which key was pressed and functions accordingly. Pressing one key alters according the situation one, two or three voltage levels in processor pins 17-19, so that these three lines have enough key combinations to be detected.
Power and shift keys are not connected to the key matrix but directly to processor pins 14 and 31. Pressing the shift-key pulls down the pin in question, from which the processor distinguishes the actions to follow.
The power key is connected to processor pin 14 through D515 and R580. A diode is needed because the normal voltage of the power line (no key has been pressed) is approx. 16V, since the line in question is connected to other functions as well, and the processor's pin in question cannot handle a voltage exceeding 5V. C535 is used to prevent the effects of disturbances to the power line and to the processor

in a start-up situation. The function of the power key (Sleep switch) has been explained more closely in the following chapter.

14.3 The power switch

The power switch (Sleep switch) operates like a normal power switch. The monitor changes its mode every time the user presses a key (and when the device is connected to power voltage). The operational information is in the non-volatile memory (EEPROM) inside the processor, so that the monitor can return to its previous mode after a power failure. Switching off the monitor from the sleep switch will not shut down the power supply, the monitor will just go to “power off” power save mode, and the led is unlit.

When the sleep switch is pressed, connector Q502 pin 9 (power) goes to the ground. Diode D126 pulls down T122 base, so that the transistor will be blocked and the 5V regulator IC103 will not get a 16V voltage. The capacitor C166 gives electricity for a brief moment to the regulator, so that for instance the processor is operating a few mS after the sleep key has been pressed. After the sleep key has been pressed, diode D515 pulls down IC501 pin 14. From this the processor determines that the sleep key has been pressed, so it alters the power bit mode in the EEPROM. If the bit was set (monitor is operational) it will be reset (monitor not operational) and vice versa. This will be done with the electricity charged in C166. After a while C166 has been discharged, so that also 5V will be cut off and the processor is shut down. By pressing the sleep key, a possible processor failing situation is also avoided, since the processor’s electricity supply is cut off. When the sleep switch is released (not pressed anymore), R140 pulls up T122 base and the transistor goes leading so that C166 is charged and 5V is back to normal. At that point, after the reset situation, the processor is operating again and reads the power bit mode in the EEPROM, and adjusts the monitor to the according mode. The processor reads the sleep key press before 5V is cut off and alters the power bit mode. Only after the regaining of 5V, the processor directs the monitor to the appropriate mode.
During a power failure (no mains power), the function is similar, but since the sleep key has not been pressed, the processor will not alter the power bit mode. When the mains power and 5V is regained, the processor sets the monitor to the same mode it was before the failure.

If an external 5V is used, the pressing of the sleep key will also pull down T540 base through D509. As a result, T502 is leading, T504 and T501 are not leading, at which time the processor cannot get supply voltage through the signal cable (EXT_5V). At that point, C166 gives electricity for a brief moment to the 5V regulator and there on to the processor through T502, so that the processor has time to alter the power bit mode. When C166 is discharged, the processor function is shut down, since the external 5V is cut off with T501. A possible failure situation of the processor is also avoided by pressing the sleep key, since the processor electricity is also cut off. When the sleep key is released, T501 goes conducting and T502 non-conducting, and the processor has regained its electricity from the external 5V and continues to operate as mentioned above.

Important!! The monitor’s power supply is operational when mains current is available. For instance, a 160V is on even if the monitor has been “shut down” from the sleep switch. When repairing the monitor the mains current must be cut off by removing the mains plug from the mains socket.

14.4 The LED control and Led_bar function

The LED control (only green led in the membrane key, in the Nokia model, the LED is in the keypad card) is totally controlled by the processor. The LED anode is connected to 5V (VXX Q502 connector pin 6). The cathode (LED signal Q502 connectors pin 7) is connected with R575 to processor IC501 pin 50. In a normal situation, when the monitor is on, pin 50 is down so the LED is lit. When the monitor is shut down from the keypad, pin 50 goes up, and the LED is unlit. In a power-off situation, pin 50 is down for a brief period but up most of the time, so the LED is blinking.
In the Nokia model, there is also a mute-LED (also on the keypad card), which is lit when the microphone mute function is operational, that is, the microphone signal will not connect forward. This LED’s control is coming from pin 38 (open collector). The LED’s anode is connected to 12V (Q502 connector pin 4). The cathode (MUTE_LED signal in Q502 connector pin 2) is connected with R599 to processor IC501 pin 38.
In the normal situation, when the mute function is not on, pin 38 is up, so that the LED is not lit. When the mute function is started, pin 38 goes down, and the LED is lit.

Additionally, the Nokia model has a LED_BAR function, where 10 LED's are in a row on the keypad card (bar display mode). These LED's show the settings mode, for instance when the user is adjusting contrast, the LED's are lit according the level of contrast. When the adjustment is in its maximum, all LED's are lit, and when the adjustment is in its minimum, all LED_BARs are unlit, which is the case also when the user has not touched the adjustments for a moment.
The LED_BAR function is done with a National Semiconductor LED control circuit LM3914, located on the keypad card. The circuit can control 10 LED's in maximum with constant current independently from the supply voltage, and needs only a few external components in addition to the LED's. The circuit supply voltage is brought from Q502 connector pin 4 (12V, J5xx only in the Nokia model), which is connected to the circuit's pin 3. The processors DAC12 (pin 34) controls through Q502 connector 8 the LM3914 pin 5, and the higher the voltage in pin 5, the more LED's are lit. Resistors R1, R2 are used to set the maximum to 5V (all LED's lit) and the LED current to approx. 10 mA. The circuits pin 9 defines the circuit function mode, when the pin is connected to ground, only one LED at a time is lit (dot display mode), and when the pin in question is connected to supply voltage, the so-called bar display mode is being used. The bar display mode is used in this particular monitor, so pin 9 is connected to the supply voltage. Capacitor C1 is a filtering component, used to prevent the possible oscillation of the circuit (a LED lit and unlit again continuously).

14.5 Other processor connections

The quartz (8 MHz), located between pins 33 (OSCin) and 32 (OSCout), and C517, C518, R533 are components required by the oscillator.

The processor supply voltage is filtered with C515 and C516, R562 forces the 5V voltage rapidly down in a voltage cut off situation, since the processor can easily be disturbed in a situation where its voltage is at 4V for a brief moment.

The processor's DACs (DAC0-17) are pulse width modulation type (PWM). Their output voltage is pulse shaped, and the pulse width defines what the DAC DC-voltage is after the RC-filtering. A wide positive pulse means a high voltage. A serial resistor and a capacitor are used for the filtering, for instance the filtering components of the width-DAC (Width, DAC7, pin 10) are R514 and C509. Additionally, since the setting in question is sensitive to a possible ripple (voltage altering), a second filtering circuit is used: R559, C528. DAC0 and DAC2 are open collectors, so they require pull-up resistors R556 and 577.

S-capacitor controls (PA0-4, pins 39-43) are open collectors, and their pull-up resistors are R357-541. R542-546 are used to delay the switch off of the S-correction FETs. Without these resistors, the S-capacitors shut down more rapidly (since it is done through low impedance transistor switch on) than switch on (since it is done through moderate impedance pull-up resistors. In this mode switch situation, all the S-capacitors might be temporarily switched off, and the dynamic focus voltage would rise very high, which is not wanted. By using serial resistors, the FET switch off is slowed down (these do not affect much the start up), so that some FET is always leading, and the dynamic focus voltage will not rise excessively.

The plugged signal (coming from the signal cable) is connected to processor pin 21. In normal function, this signal is grounded (pin 21 down) by the computer video card, and the monitor is functioning normally. When the signal cable is removed, processor pin 21 is pulled up by the internal pull-up resistors. The processor determines that this is a so called self-test situation. As a result, it starts to form horizontal and vertical pulses by itself (since there are none coming from the removed signal cable), increases slightly the G2-control voltage and sets the brightness to maximum. The monitor is thus functioning on constant frequency (approx. 64 kHz and 74 kHz) and shows a self test screen (a bright frame image), from which the user can deduct that the monitor is functioning normally.

The monitor has a protection against failing situations, if the horizontal or vertical output stage is damaged. In such a situation, the picture tube phosphor can be damaged because the beam current is concentrated on very small phosphor area.
The protection against the damaging of the horizontal stage is automatic, because if the stage in question is damaged, there is no horizontal fly-back pulse available. This pulse keeps the high voltage generator operational, so if the horizontal stage is damaged, also the high voltage disappears and the picture tube remains intact.
The damaging of the vertical stage is prevented with an internal protection program of the processor. The processor is constantly examining if there is an incoming vertical fly-back pulse (V_FLY signal,

processor pin 20), if not, the processor interprets it as a failure situation and sets the monitor to Power Off-mode (the led is not blinking in this situation), that is, cuts off the electricity from the deflection stages, at which point the high voltage is cut off. The above mentioned situation occurs also if the deflection coil connector is not in place, since there is no incoming vertical fly-back pulse.

Additional memory IC504 (EEPROM) is connected through the IIC-line. The memory is not in use in the basic device. The bus goes from processor pins 53 (SCL) and 54 (SDA). According the DDC definition, an external supply voltage can be brought to the processor through the signal cable connector.

Transistors T501, T502 and T504 switch on the external voltage (EXT_5V) if available, and if the voltage from the monitor's own supply source (5V) is under 4.6V. This function is not operational in the basic device, and the external 5V is thus not used. The function of the circuit is based on regulator T503, which is leading if its control voltage is under 2.5V. D509 ensures the momentary cut-off of the processor voltage and the reset generating by pressing the power switch, even if external voltage would be available. As a result, by pressing the power switch, the processor can recover from a possible failure situation without having to shut down the computer.

15 The video amplifier

The video amplifier is composed of a three-channel pre-amplifier, a three-channel output amplifier, three black level adjustment and clamping circuits, and three brightness adjustment circuits. The video amplifier is designed to control a 17" picture tube under 100 MHz dot frequency. From the video amplifier settings, brightness, contrast, minimum contrast, maximum contrast and amplitude settings are adjusted through a DC-control voltage coming from the base board (processor DAC adjustment voltage). Trimmers are used for the black level adjustments.

15.1 The pre-amplifier

The used pre-amplifier is a three-channel National LM1207 circuit, with a band-width of 85 MHz. The pre-amplifier circuit contains an input amplifier, a contrast adjustment stage, a keyed black level clamp circuit, an adjustable amplifier stage and an output circuit. The circuit operates with a 12V supply voltage.

The video signals, which are outputted to 75 ohm output resistors, are brought through switching capacitors C101, C201 and C301 to the circuits input pins 4, 6 and 9. The input pins are pre-amplified to 2.8V with the internal reference voltage.

The contrast adjustment voltage is brought to the circuit's pin 12, and it is adjustable to 0…32V. The contrast adjustment voltage adjusts the amplifying of the three channels at the same ratio, at which time the color shade remains the constant contrast adjustment function.

A negative polarity black level clamp keying pulse is brought from connector Q2 pin 15, and directed to the circuits pin 14. The keying pulse is in the same time period as the line sync pulse. During the keying, the circuit compares the output DC-level to the adjusted reference level and corrects it to the right level. The reference voltage done with resistors R6, R7 and R14 is taken to the circuits pins 16, 19 and 27.

A negative polarity line blanking pulse is brought from connector Q2 pin 12 to the amplifiers pin 13. The circuit outputs are switched to ground during the blanking pulse.

The internal reinforcement of the circuit channels is adjustable as DC adjustments through pins 15, 18 and 28. The G-channel adjustment voltage (pin 18) has been set to constant with resistors R2 and R3. The adjustment voltages of R and B channels are brought to the pre-amplifier through processor connector Q2 pins 14 and 13. The adjustment range of the adjustment voltages is 0…4V. The white picture color balance can be optimized with amplifying adjustments.

Output signals are brought from circuit output pins 17, 20 and 26, with an amplitude of 2-3V as the contrast is at maximum, and the black similar levels are approx. 1V. During the line blanking the outputs are approx. at 0V. The output signal is directed through resistors R105, R205 and R305 to the output stage input.

15.2 The output stage

The used output stage is a National three-channel monolithic circuit LM2405. The amplifier is a cascade amplifier equipped with an active load stage, and with a voltage amplifying of approx. 14 (23dB). The output stage input is DC-switched, and the output of the preamplifier biases the output stage so that the voltage corresponding to black is approximately 60V at the output stage's output. During the blanking, the output rises near 70V. The output stage operates with a 70V supply voltage. The output stage output is AC-connected.

The video signals are brought from the pre-amplifiers outputs to the output stage IC410 inputs 9, 8 and 11 (R, G and B). RC-chains R106, C102, R206, C202, R306 and C302 are used to correct the smearing errors in the output stage. A 12V bias voltage is brought to the output stages pin 10, and a filtered supply voltage (70V) to its pin 6. Approx. 35V amplitude signals are obtained from the output stages pins 3, 5 and 1, and directed through switching capacitors C120, C220 and C320 to the black level clamping.

15.3 The black level clamp and adjustment circuit

After coupling capacitors C120, C220 and C320, the video signal black levels must be clamped on each channel, so that the background (frame) color balance is right. An non-keyed diode clamping is used in the black level clamping.

The cathode black levels are adjusted with trimmers RT120, RT220 and RT320. The adjustment voltage from trimmer RT120 (R-channel) directs the transistor T120 base functioning as current generator. The black level proportional adjustment voltage brought from the transistor collector is buffered with transistor T122. The line sync pulse period video signal level is clamped with diode D123 to the voltage in transistor T122's emitter. The most sensitive cathode black level is approx. 95V, just when the frame has been adjusted just invisible with the brightness adjustment.

After the black level clamp, video signals are directed through parallel peaking circuit L120, R129 (R-channel), and protector resistor R131 to the cathodes.

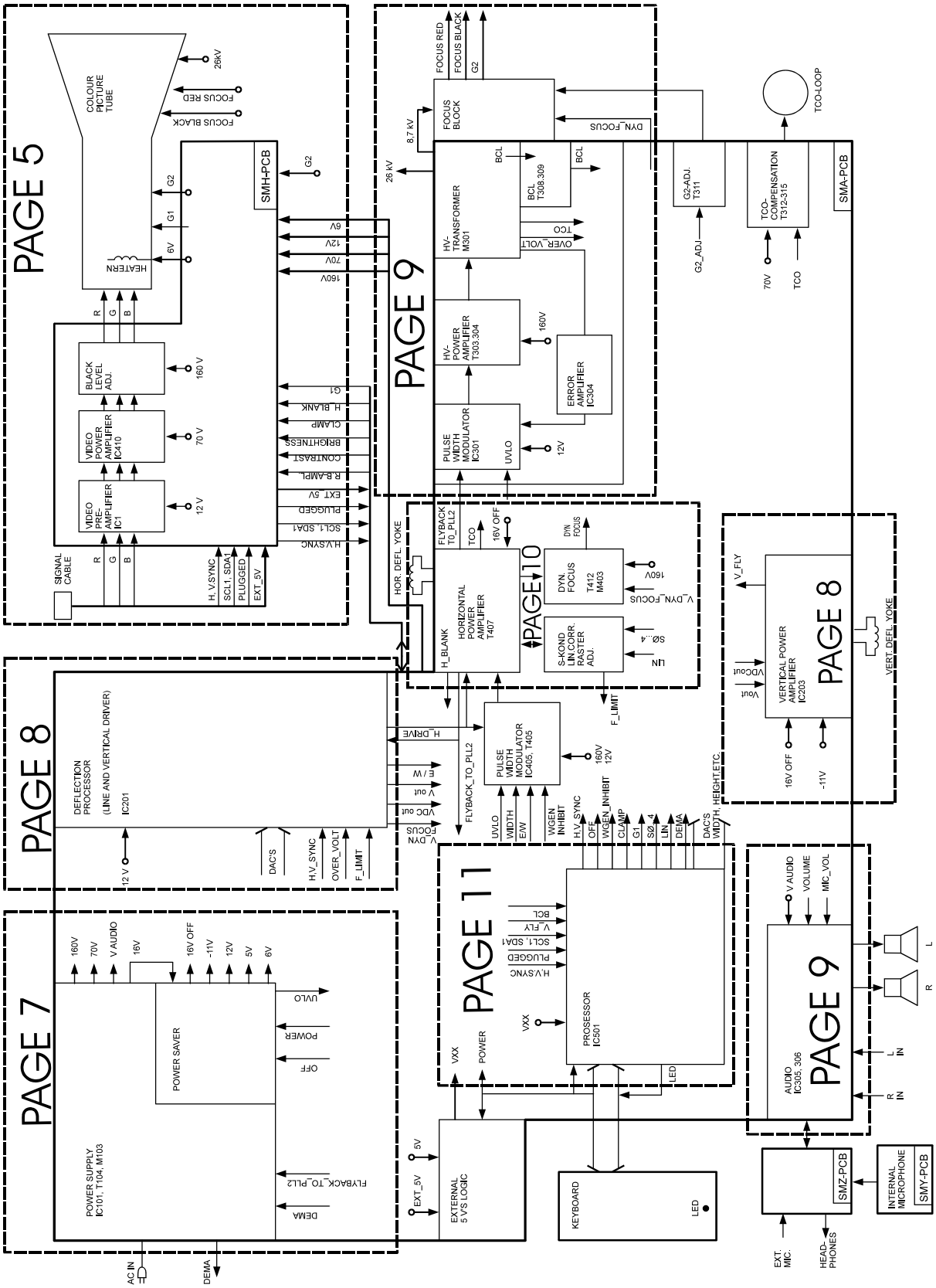
15.4 The brightness adjustment circuit

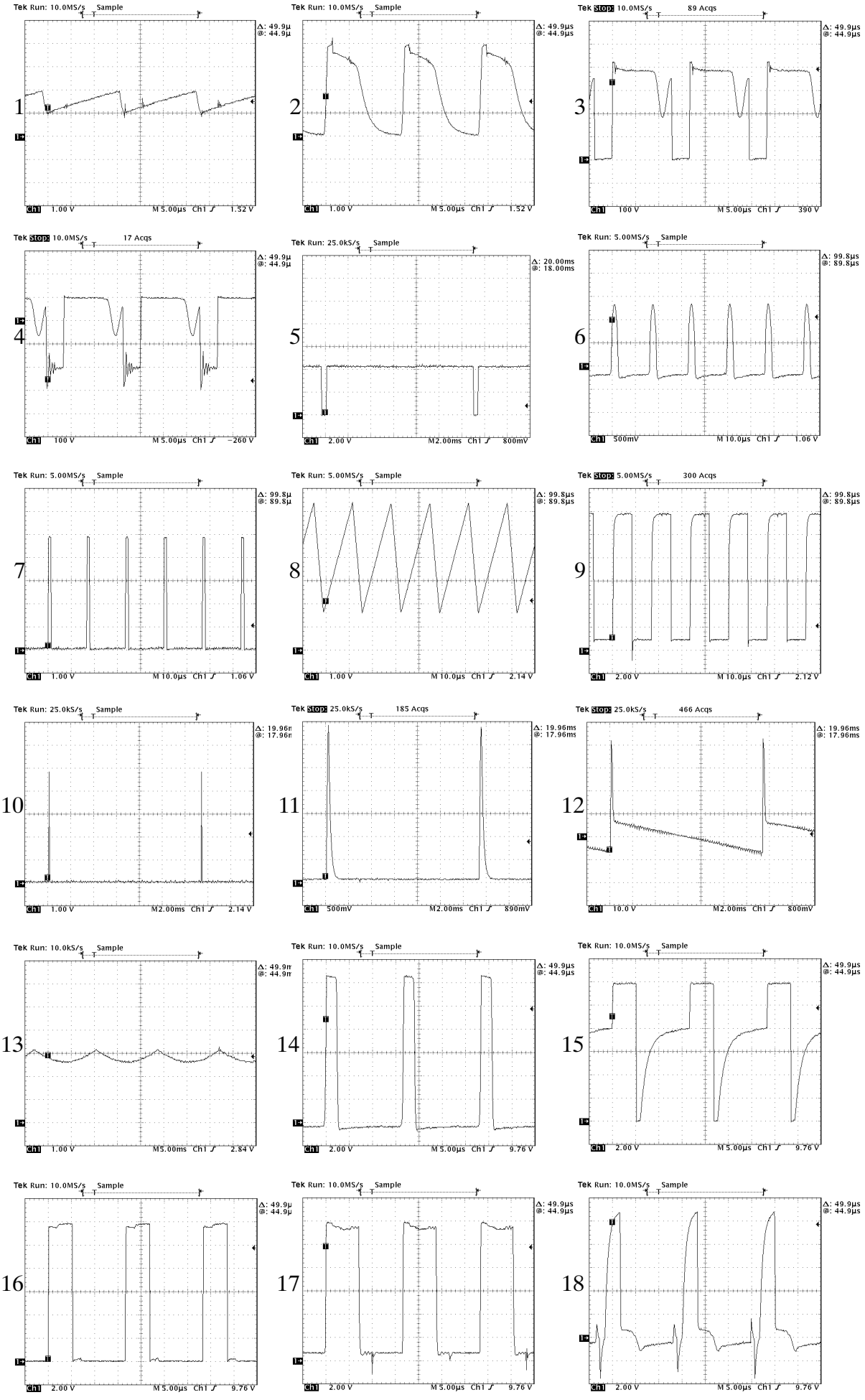
Brightness adjustment is used to adjust the cathodes' black level voltages through black level adjustment circuits, emphasized with typical amplitudes of the channels, at which time the color temperature remains as the proper brightness function.

The brightness adjustment voltage 0…5V brought from connector Q2 pin 16 is buffered with transistor T60 and directed to transistors T121, T221, T321 bases, functioning as current generators. The transistors' collector currents alter the base voltage of transistors T122, T222 and T322, and thus also the black level voltage on the cathode. The channel brightness adjustment voltage emphasizing is obtained with resistors R123, R223, R224, R323 and R324.

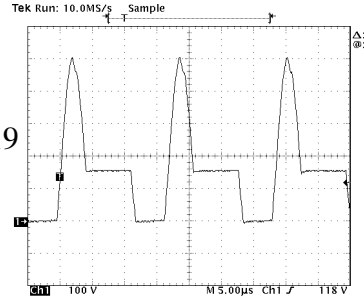
The summed adjustment range of the black level and brightness adjustment is approximately 60…105V.

BLOCK DIAGRAM




Tek Run: 10.0MS/s Sample
Δ: 49.9µ
@: 44.9µ
1
Ch1 1.00 V M 5.00µs Ch1 1.52 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µs
@: 44.9µs
2
Ch1 1.00 V M 5.00µs Ch1 1.52 V
Tek Stop: 10.0MS/s 89 Acqs
Δ: 49.9µs
@: 44.9µs
3
Ch1 100 V M 5.00µs Ch1 390 V
Tek Stop: 10.0MS/s 17 Acqs
Δ: 49.9µ
@: 44.9µ
4
Ch1 100 V M 5.00µs Ch1 −260 V
Tek Run: 25.0kS/s Sample
Δ: 20.00ms
@: 18.00ms
5
Ch1 2.00 V M2.00ms Ch1 800mV
Tek Run: 5.00MS/s Sample
Δ: 99.8µs
@: 89.8µs
6
Ch1 500mV M 10.0µs Ch1 1.06 V
Tek Run: 5.00MS/s Sample
Δ: 99.8µ
@: 89.8µ
7
Ch1 1.00 V M 10.0µs Ch1 1.06 V
Tek Run: 5.00MS/s Sample
Δ: 99.8µs
@: 89.8µs
8
Ch1 1.00 V M 10.0µs Ch1 2.14 V
Tek Stop: 5.00MS/s 300 Acqs
Δ: 99.8µs
@: 89.8µs
9
Ch1 2.00 V M 10.0µs Ch1 2.12 V
Tek Run: 25.0kS/s Sample
Δ: 19.96m
@: 17.96m
10
Ch1 1.00 V M2.00ms Ch1 2.14 V
Tek Stop: 25.0kS/s 185 Acqs
Δ: 19.96ms
@: 17.96ms
11
Ch1 500mV M2.00ms Ch1 890mV
Tek Stop: 25.0kS/s 466 Acqs
Δ: 19.96ms
@: 17.96ms
12
Ch1 10.0 V M2.00ms Ch1 800mV
Tek Run: 10.0kS/s Sample
Δ: 49.9m
@: 44.9m
13
Ch1 1.00 V M5.00ms Ch1 2.84 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µs
@: 44.9µs
14
Ch1 2.00 V M 5.00µs Ch1 9.76 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µs
@: 44.9µs
15
Ch1 2.00 V M 5.00µs Ch1 9.76 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µ
@: 44.9µ
16
Ch1 2.00 V M 5.00µs Ch1 9.76 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µ
@: 44.9µ
17
Ch1 2.00 V M 5.00µs Ch1 9.76 V
Tek Run: 10.0MS/s Sample
Δ: 49.9µs
@: 44.9µs
18
Ch1 2.00 V M 5.00µs Ch1 9.76 V

19



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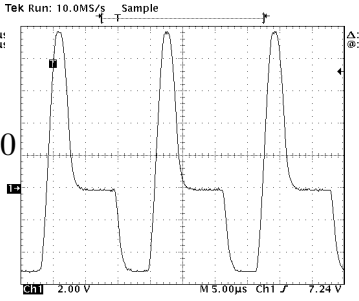

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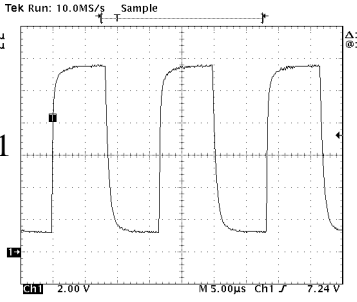

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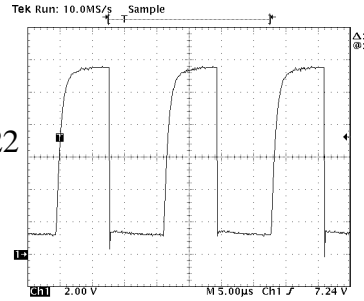

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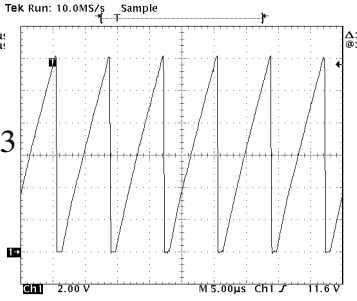

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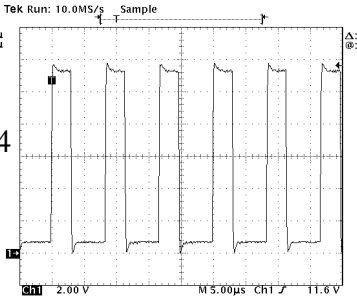

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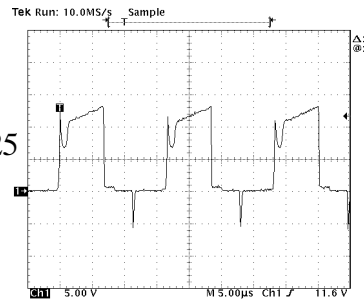

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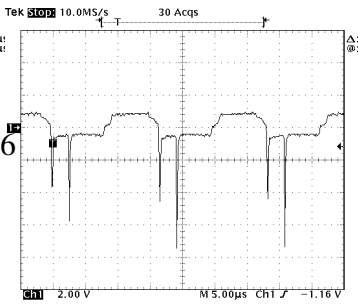

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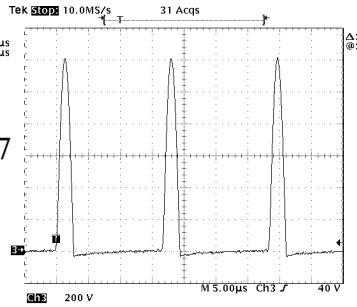

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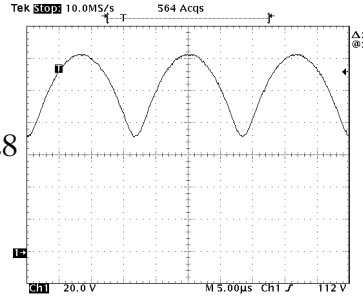

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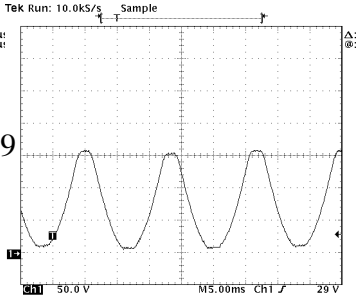

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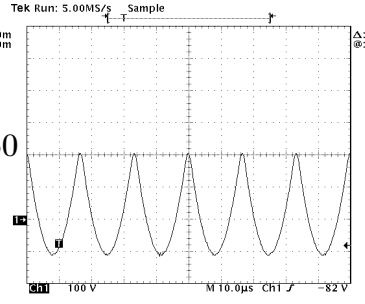

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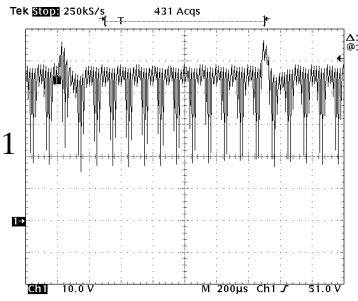

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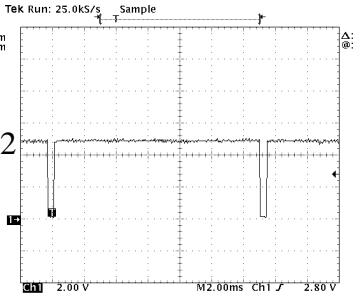

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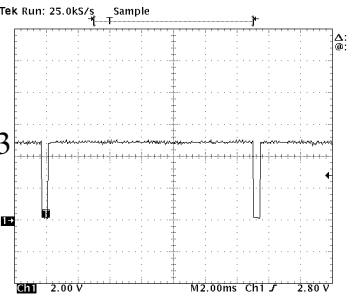

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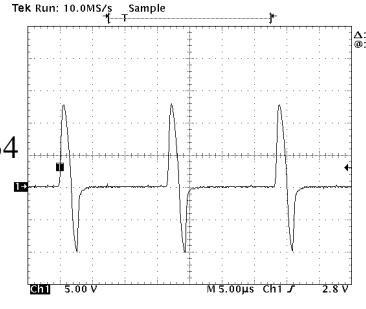

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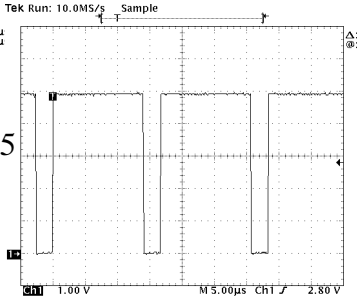

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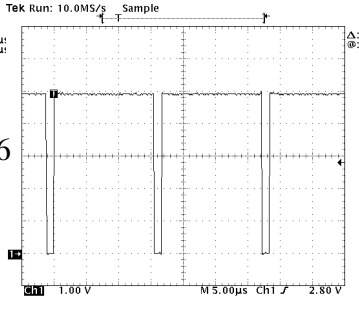
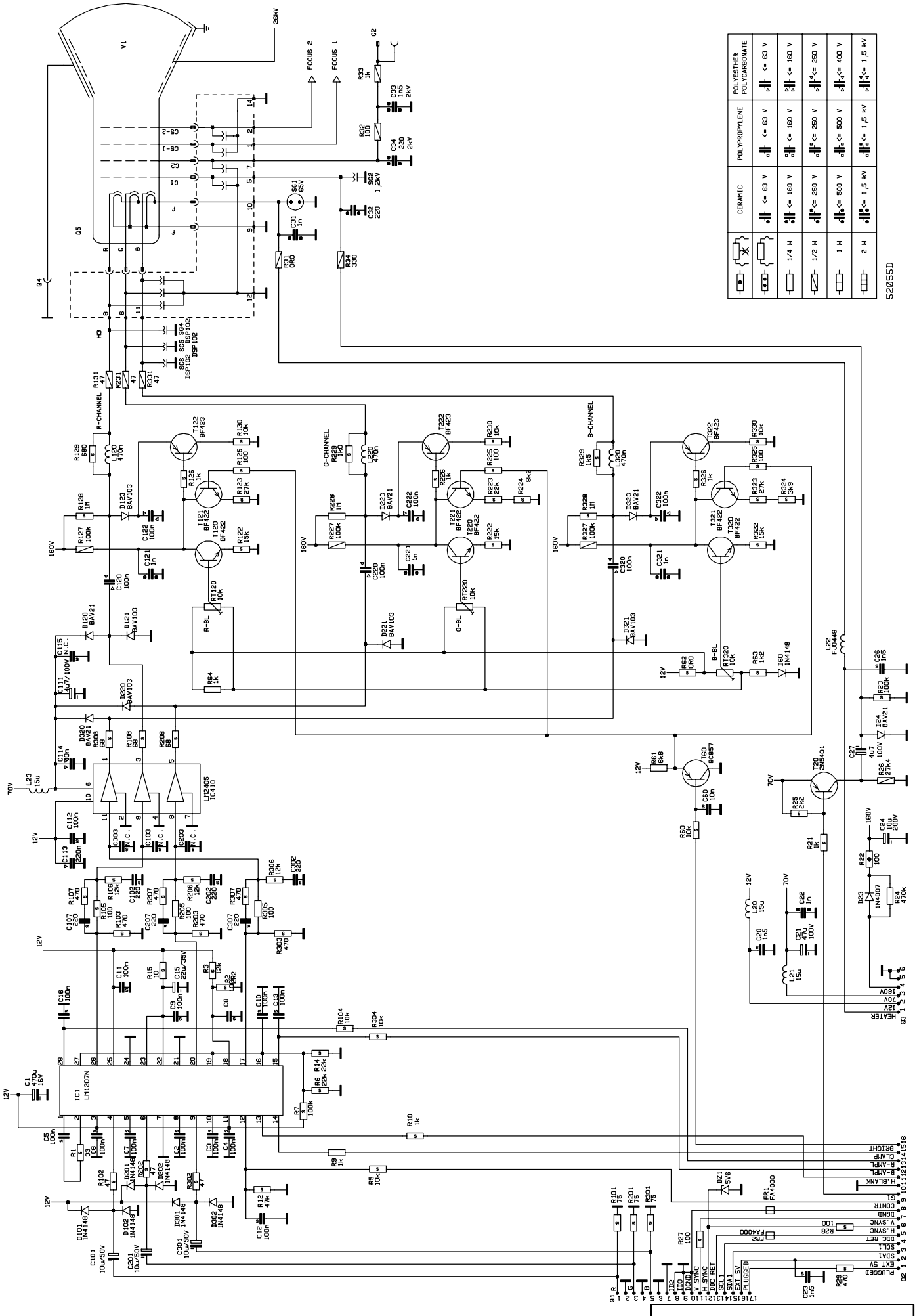
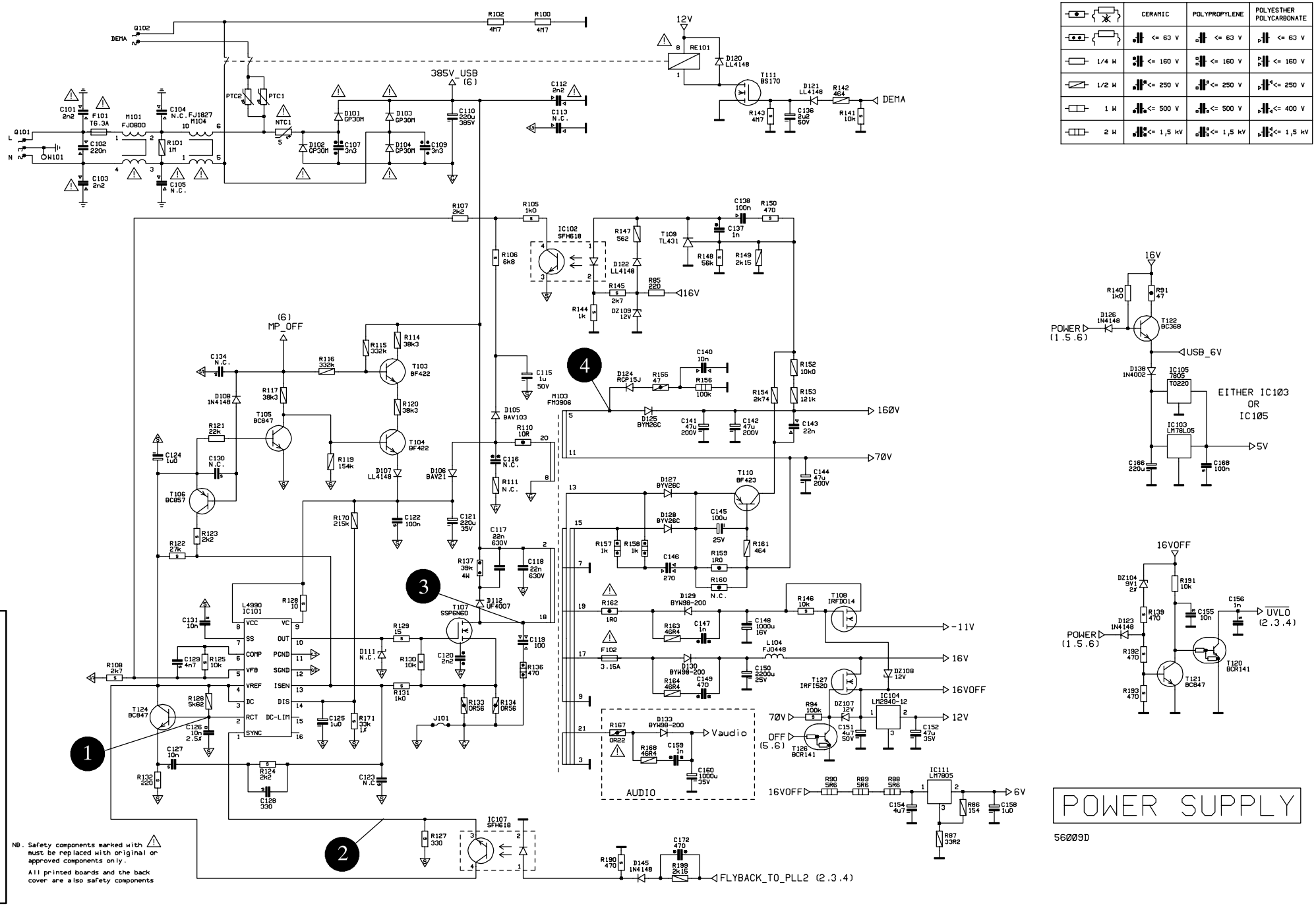



SMH143D
D3117D 02.97 Page 5
447Z



	CERAMIC	POLYPROPYLENE	POLYESTHER POLYCARBONATE
	<= 63 V	<= 63 V	<= 63 V
1/4 W	<= 160 V	<= 160 V	<= 160 V
1/2 W	<= 250 V	<= 250 V	<= 250 V
1 W	<= 500 V	<= 500 V	<= 400 V
2 W	<= 1,5 kV	<= 1,5 kV	<= 1,5 kV

NB. Safety components marked with ⚠ must be replaced with original or approved components only.

All printed boards and the back cover are also safety components

POWER SUPPLY

56009D

SMA187D/198D

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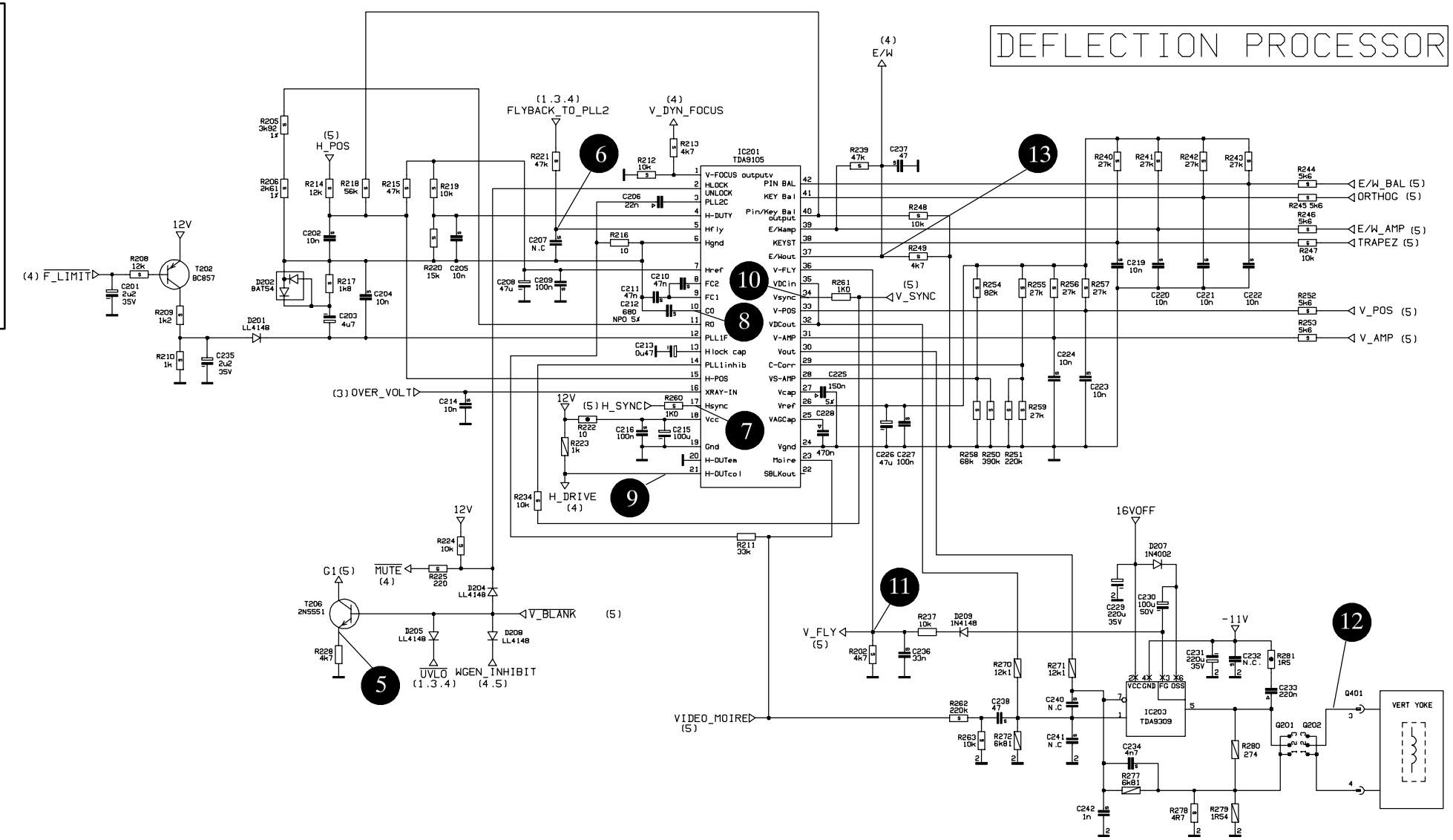
447Z

DEFLECTION PROCESSOR

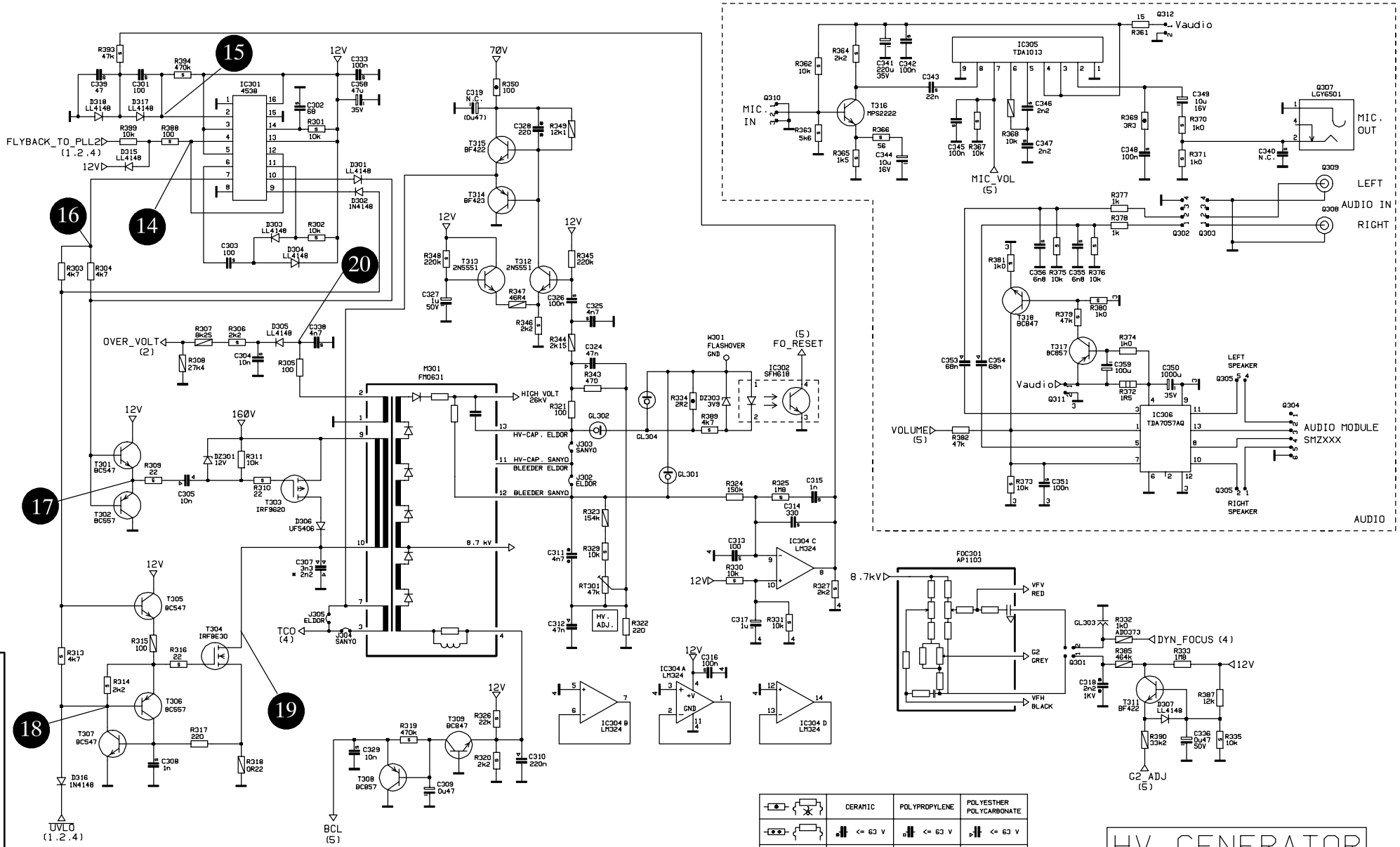


	CERAMIC	POLYPROPYLENE	POLYESTHER POLYCARBONATE
	<= 63 V	<= 63 V	<= 63 V
1/4 W	<= 160 V	<= 160 V	<= 160 V
1/2 W	<= 250 V	<= 250 V	<= 250 V
1 W	<= 500 V	<= 500 V	<= 400 V
2 W	<= 1,5 kV	<= 1,5 kV	<= 1,5 kV

VERT. OUTPUT

56009D

447Z



447Z

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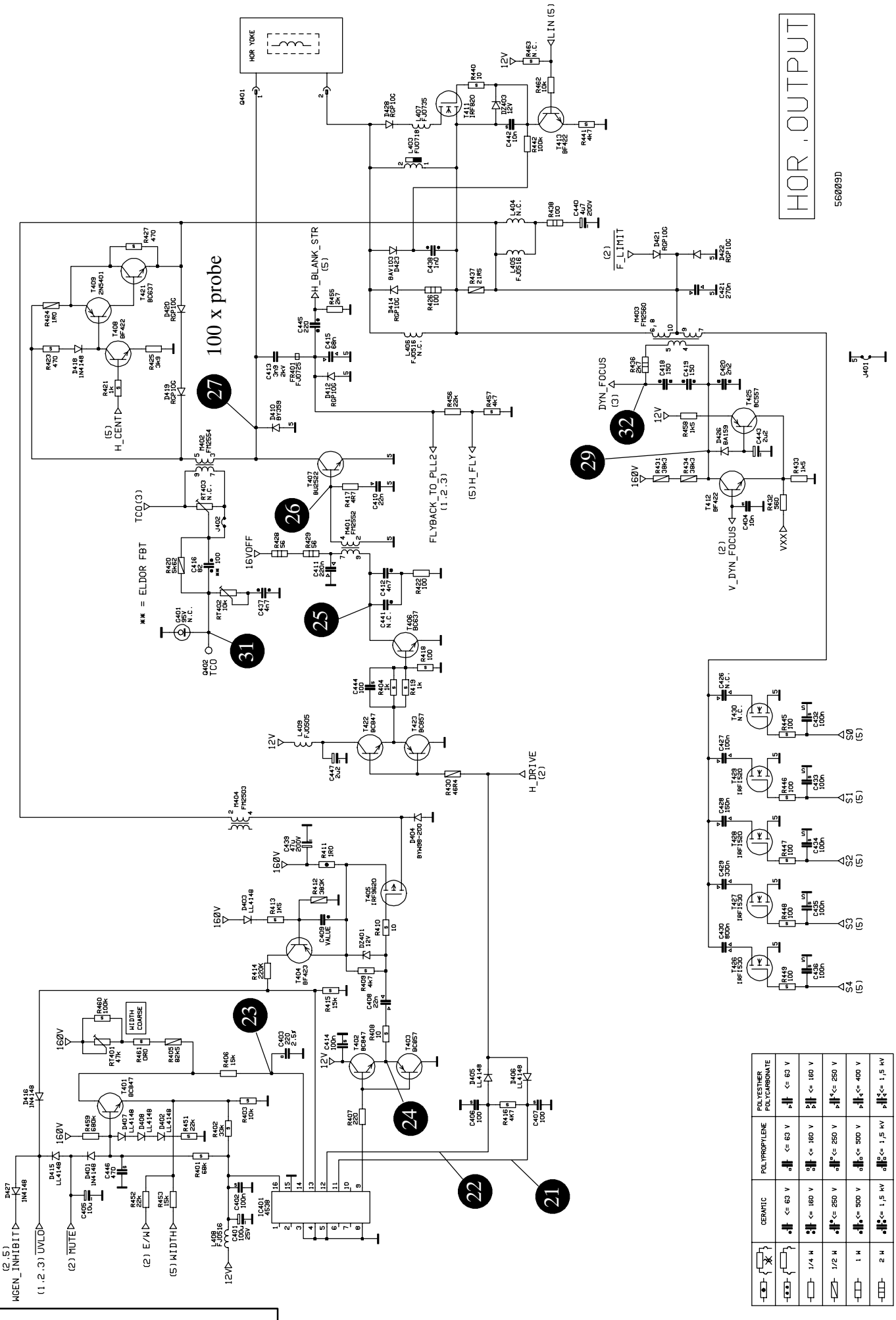
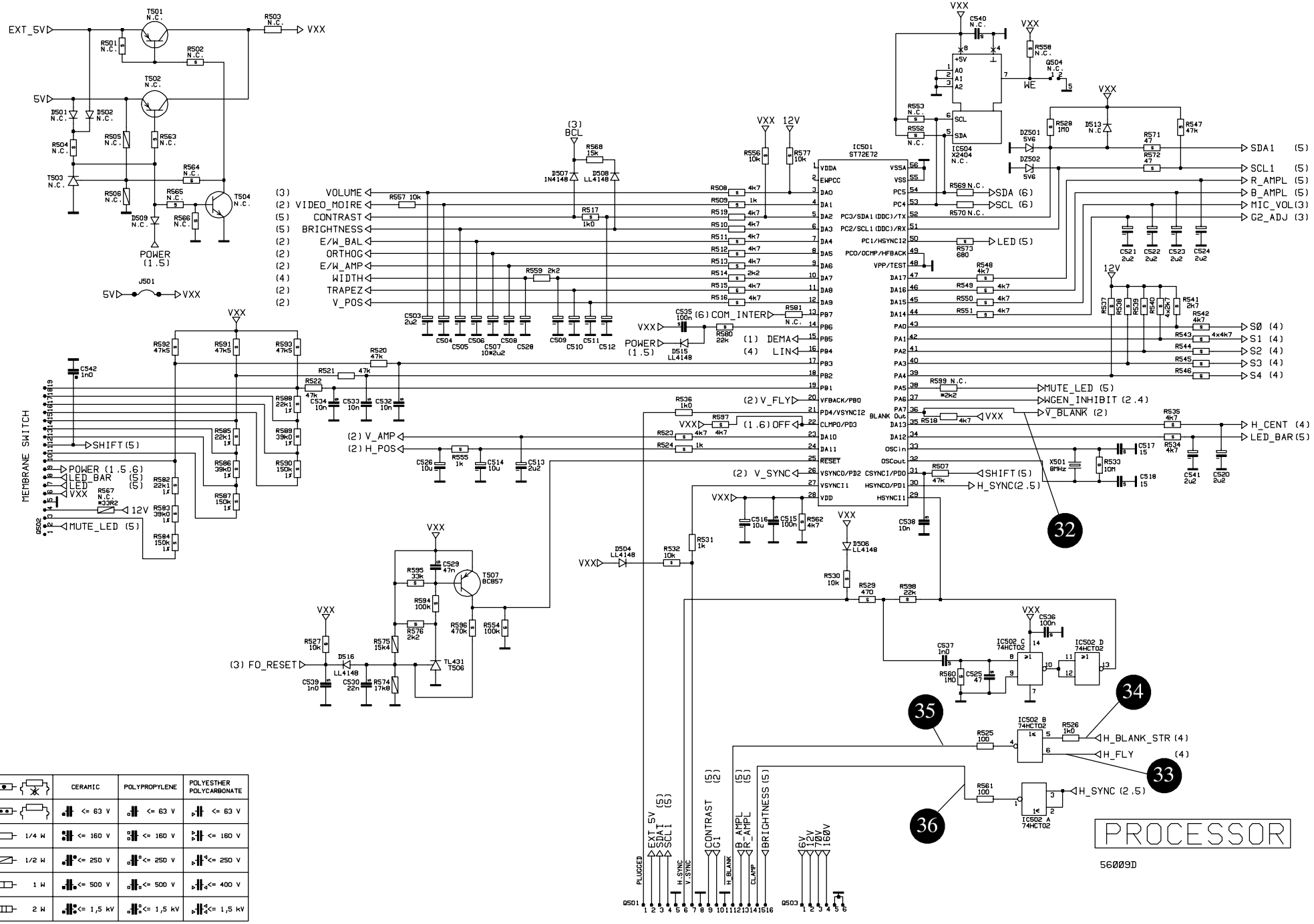
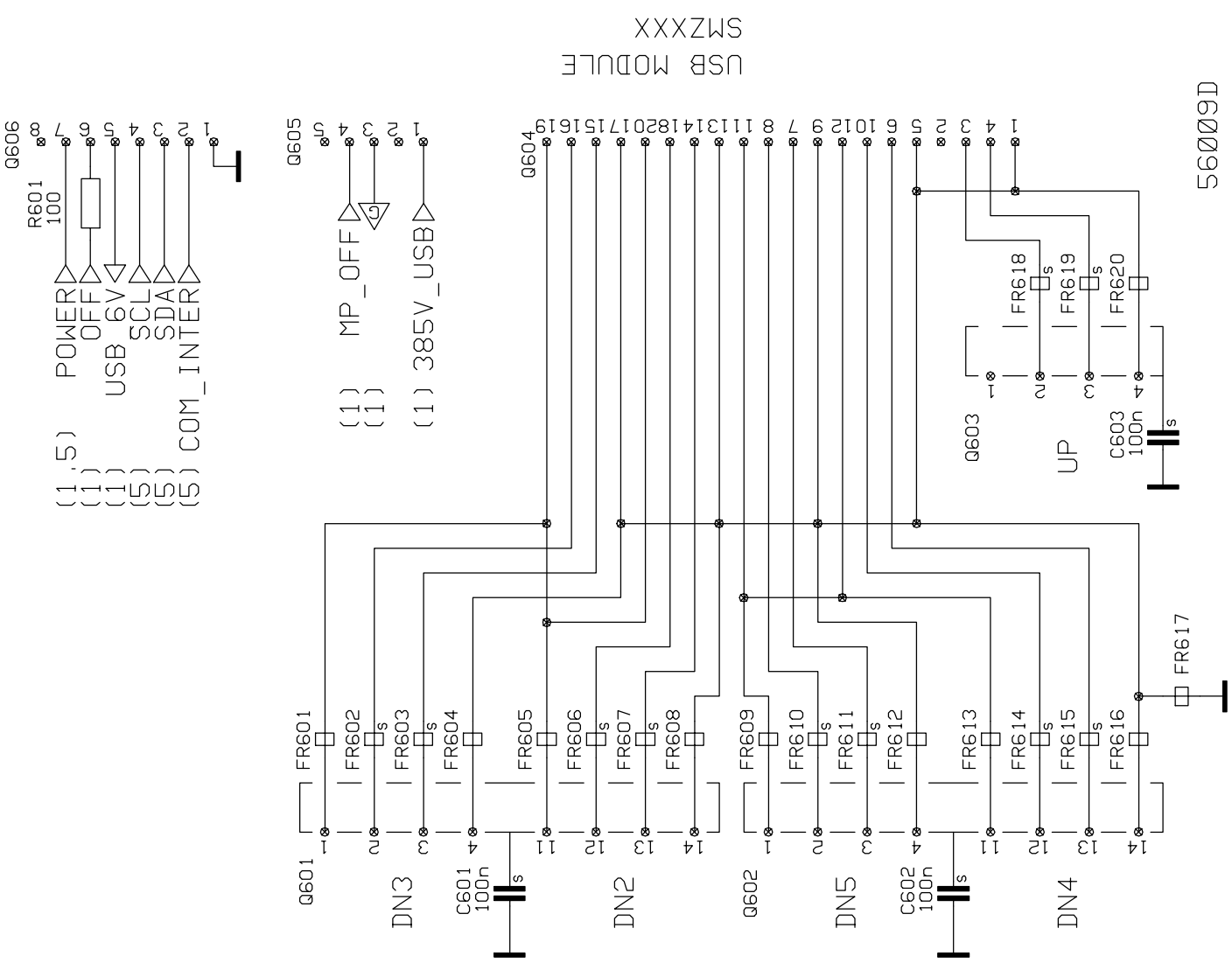

HOR. OUTPUT
56009D
100 x probe
HOR YOKE
H_BLANK_STR
(5)
F_LIMIT
(2)
DYN_FOCUS
(3)
H_CENT
(5)
FLYBACK_TO_PLL2
(1.2.3)
(5)H_FLY
TCO(3)
16VOFF
** = ELDOR FBT
H_DRIVE
(2)
V_DYN_FOCUS
(2)
VXXX
WGEN_INHIBIT
(2,5)
UVLO
(1.2.3)
MUTE
(2)
E/W
(2)
WIDTH
(5)
WIDTH COARSE
CERAMIC
POLYPROPYLENE
POLYESTHER
POLYCARBONATE
1/4 W
1/2 W
1 W
2 W


SMA187D/198D
D3116D 02.97 Page 11
447Z
PROCESSOR
56009D
CERAMIC
POLYPROPYLENE
POLYESTHER POLYCARBONATE
IC501 ST72E72
IC504 X2404 N.C.
IC502 A 74HCT02
IC502 B 74HCT02
IC502 C 74HCT02
IC502 D 74HCT02
MEMBRANE SWITCH
VOLUME
VIDEO_MOIRE
CONTRAST
BRIGHTNESS
E/W_BAL
ORTHOG
E/W_AMP
WIDTH
TRAPEZ
V_POS
COM_INTER
DEMA
LIN
V_FLY
V_AMP
H_POS
OFF
V_SYNC
SHIFT(5)
H_SYNC(2,5)
MUTE_LED (5)
WGEN_INHIBIT (2,4)
V_BLANK (2)
H_CENT (4)
LED_BAR(5)
SDA1 (5)
SCL1 (5)
R_AMPL (5)
B_AMPL (5)
MIC_VOL(3)
G2_ADJ (3)
S0 (4)
S1 (4)
S2 (4)
S3 (4)
S4 (4)
SDA (6)
SCL (6)
LED (5)
FO_RESET
H_BLANK_STR (4)
H_FLY (4)
32
33
34
35
36


USB MODULE
SMZXXX
560090
Q606
R601
100
(1,5) POWER
(1) OFF
(1) USB_6V
(5) SCL
(5) SDA
(5) COM_INTER
Q605
(1) MP_OFF
(1)
(1) 385V_USB
Q604
Q603
FR618
FR619
FR620
UP
C603
100n
FR617
Q601
FR601
FR602
FR603
FR604
FR605
FR606
FR607
FR608
DN3
C601
100n
DN2
Q602
FR609
FR610
FR611
FR612
FR613
FR614
FR615
FR616
DN5
C602
100n
DN4